KElm-A5ESoM
Hardware Manual

Ver.1.0

Kondo Electronics Industry Co., Ltd.

Introduction

Thank you for purchasing a KEIm product.
Read this manual and related document thoroughly before using this product and observe the precautions for use.

CAUTION

- The contents of this manual are subject to change without prior notice. Contact the Kondo Electronics Industry service center or check the Kondo Electronics Industry website for the latest information before using the product.
- This product contains general electronic components. Do not use the product for devices that require extremely high reliability (aerospace equipment, nuclear power equipment, medical equipment for life support, etc.).
- This product is developed and manufactured for use only in Japan. If this product or a product that incorporates this product is exported outside Japan, all the necessary procedures must be completed at the responsibility and expense of the customer in accordance with the Foreign Exchange and Foreign Trade Act and other export laws and regulations.
- Be sure to turn off the power before inserting or removing cables to connectors other than LAN and USB.
- Do not use this product in locations subject to large amounts of water, humidity, dust, or oil smoke.
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Contact Information

- For any questions about this product, contact the following email address:

keim-support@kd-group.co.jp

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1. Overview

This manual describes the hardware specifications of the KEIm-A5ESoM, a System-on-Module (SoM) equipped with Agilex™ 5 FPGA & SoC E-Series.

1.1. Product Features

This product is a small FPGA platform powered by Agilex™ 5 FPGA & SoC E-Series. In addition to the SoC FPGA, the module features LPDDR4 SDRAM for memory, an eMMC or microSD card for storage, and QSPI flash for configuration ROM.

① Equipped with FPGA
Utilizing FPGA features such as ultra-low latency and parallel processing, it is an ideal component for product development of edge devices essential for IoT.

② Small form factor
Because the module footprint is small, it is effective for miniaturizing final products and differentiating product designs.

③ Necessary and sufficient components
The functions implemented in the SoM are kept to the minimum necessary, resulting in an efficient and highly flexible configuration. Due to its simple configuration, it is a highly reliable and stable module.

④ Long product life
It is a long-term supply component that can be used with confidence in products with long life cycles such as industrial equipment.

This product is in the form of a SoM and is intended for customers to develop and integrate carrier boards for specific purposes. By using this product as is for the core processor, which takes time to design, and developing a carrier board for each application, the product development period can be shortened.

1.2. **SoM Specifications**

Table 1-1 SoM Specifications

Item		Description
SoC FPGA		Agilex™ 5 FPGA & SoC E-Series
	Device	A5ED065BB32AE5SR0
	Processor	Dual-core Arm Cortex-A76, Dual-core Arm Cortex-A55
	Logic Elements / Adaptive logic modules	656 kLEs / 222,400 ALMs
	M20K memory blocks / size	1,611 blocks / 31.46 Mbits
	MLAB memory count / size	8,440 count / 6.79 Mbits
	I/O PLL	8
	Fabric-feeding I/O PLL	13
	Variable-precision DSP blocks	846
	18 x 19 multipliers	1,692
LPDDR4 SDRAM		4GByte (1G x 32bit) x3 MT53E1G32D2FW-046 (Micron)
QSPI Flash		256MByte (2Gbit) MT25QU02GCBB (Micron)
eMMC		32GByte MTFC32GAZAQHD (Micron)
SD		microSD Card Slot
Clock	OSC	100MHz
	Clock Generator	Low-Jitter 4-Output Clock Generator Si5340B-D-GM (Skyworks)
BtoB Connector		400-pin BtoB Connector x2
	Connector	ADF6-100-03.5-L-4-2-A (Samtec)
	HPS-IO	Ethernet (RGMII) x1, USB OTG (ULPI) x1, UART x1, I2C x1, QSPI x1, GPIO up to 21 (Depends on HPS configuration)
	HSIO	Up to 96
	HVIO	Up to 120
	Transceiver (17 Gbps)	24 lanes
	Debug I/F	JTAG
Power supply		+5V±5% (4.75V～5.25V), VCCIO (Depends on configuration)
Power consumption		TBD
Operating temperature		-25°C~ +85°C
Dimensions		118×77mm

1.3. **Block Diagram**

The Block Diagram of this product is shown in Figure 1-1.

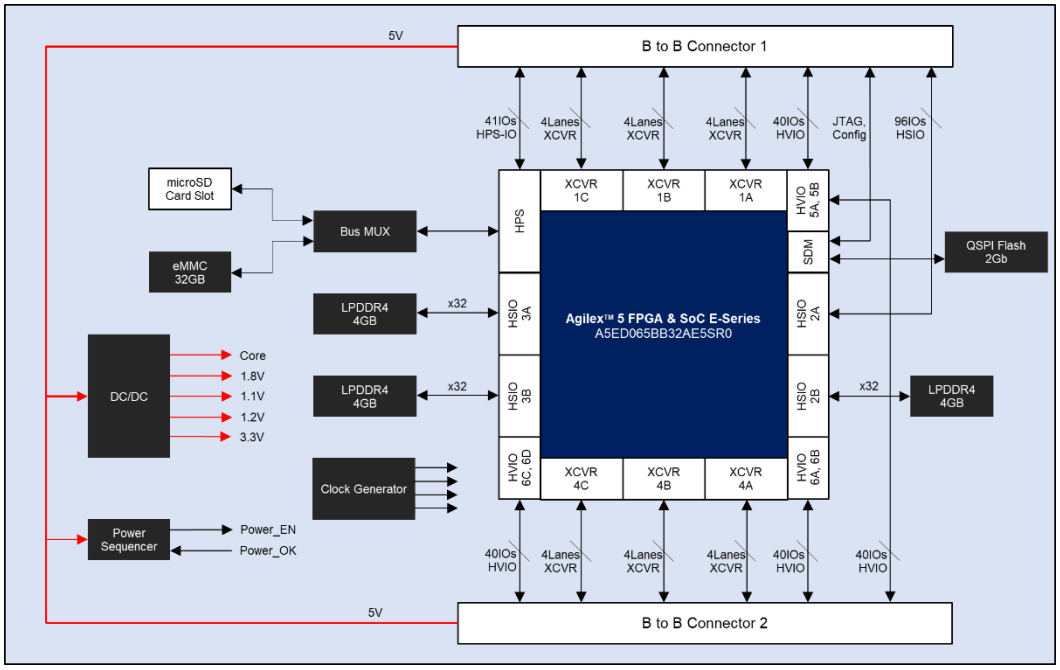


Figure 1-1 SoM Block Diagram

1.4. **Board Layout**

Figure 1-2 shows the Board Layout of the SoM, and Table 1-2 lists the Major Components installed on the SoM.

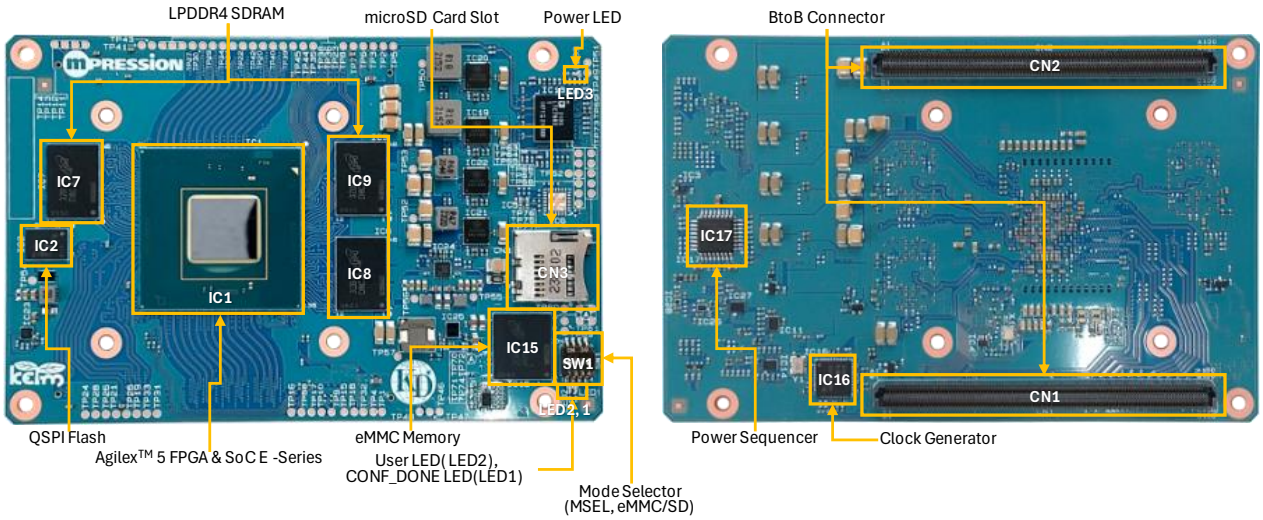


Figure 1-2 SoM Board Layout

Table 1-2 List of Major Components

Reference	Name	Description
IC1	SoC FPGA	Agilex™ 5 FPGA & SoC E-Series Device Group B A5ED065BB32AE5SR0: 1591-pin BGA
IC2	QSPI Flash Memory	MT25QU02GCBB8E12-0SIT (Micron)
IC7, IC8, IC9	LPDDR4 SDRAM	MT53E1G32D2FW-046WT:B (Micron)
IC15	eMMC	MTFC32GAZAQHD-IT (Micron) Allows you to use by switching with microSD card.
IC16	Clock Generator	Si5340B-D-GM (Skyworks)
IC17	Power Sequencer	ADM1168ASTZ (Analog Devices)
CN1, CN2	BtoB Connector	ADF6-100-03.5-L-4-2-A (Samtec) 400-pin, 0.635 mm pitch 4row socket
CN3	microSD Card Slot	Allows you to use by switching with eMMC.
LED1	CONF_DONE LED	On when FPGA configuration is done.
LED2	User LED	Controlled by HPS GPIO, ON at Low.
LED3	Power LED	On when 5V power input is applied.
SW1	Mode Switch	DIP switch for SoM operating modes.

2. Circuit Block Details

2.1. Power Supply Circuit

Figure 2-1 shows the configuration of the Power Supply Circuit of this product.

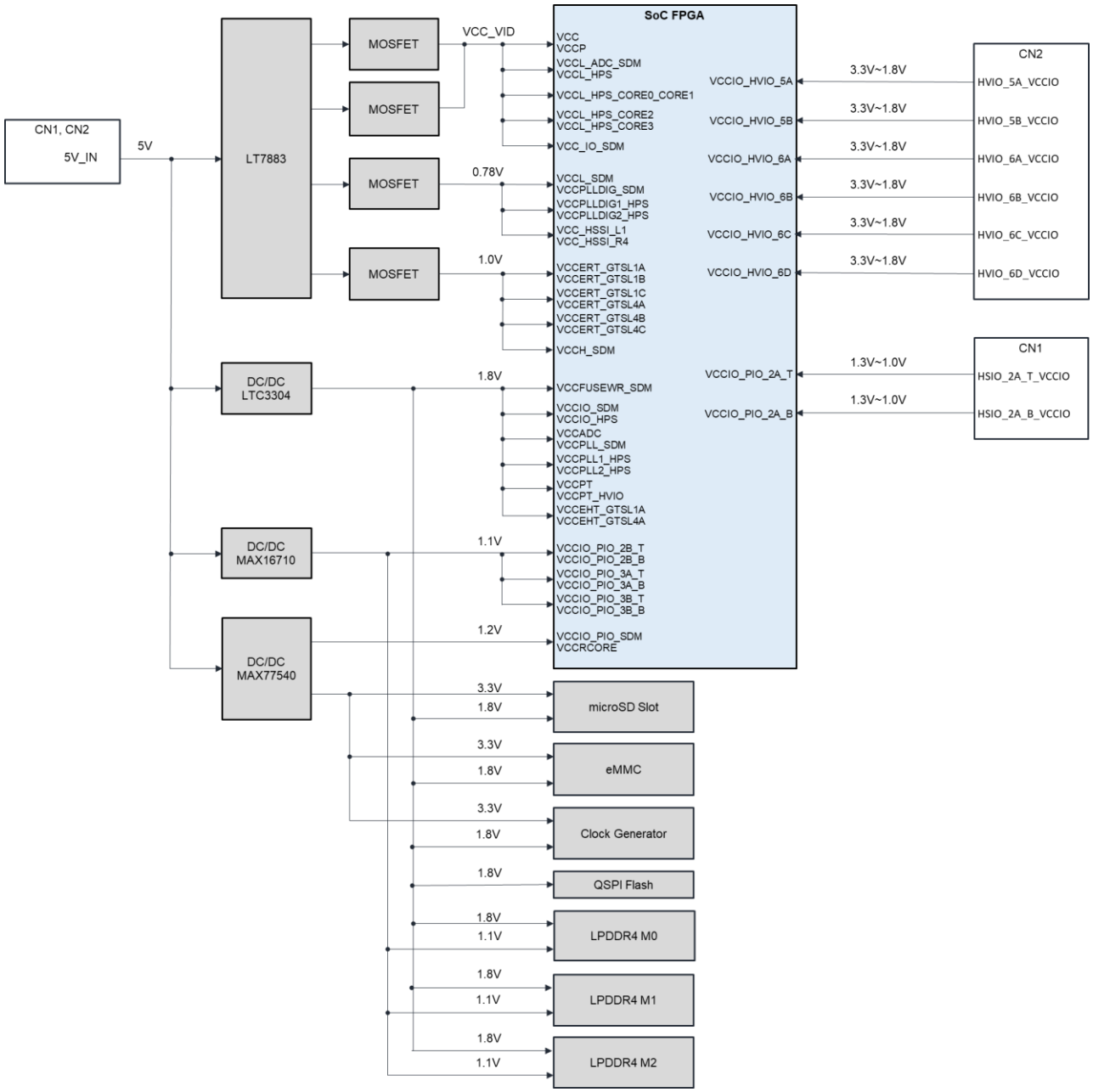


Figure 2-1 Power Supply Circuit

2.1.1. **Power-Up Sequence**

Figure 2-2 shows the Power-Up Sequence of this product.

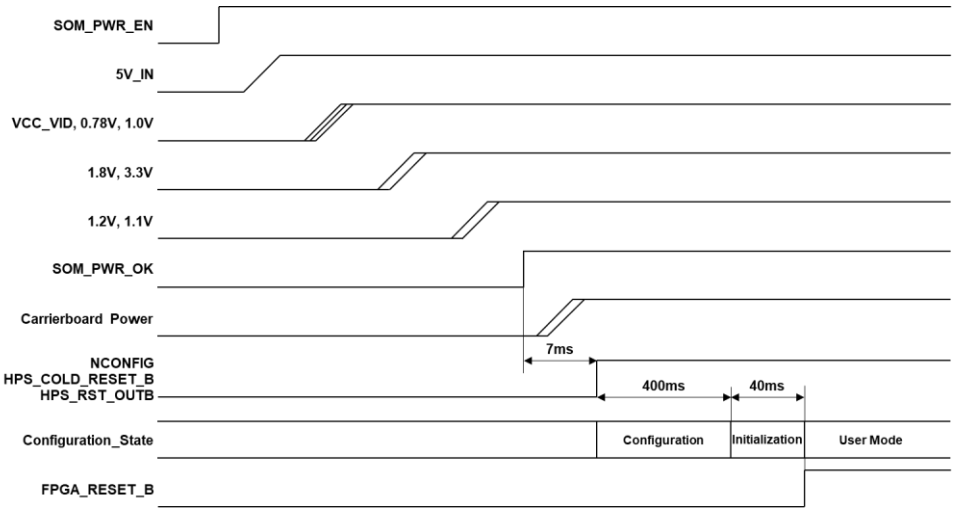


Figure 2-2 Power-Up Sequence

Important: After the SOM_PWR_OK signal output from the SoM goes High, apply voltage to the VCCIO power supply and each IO pin externally to the SoM.

2.1.2. **Power-Down Sequence**

Figure 2-2 shows the Power-Down Sequence of this product.

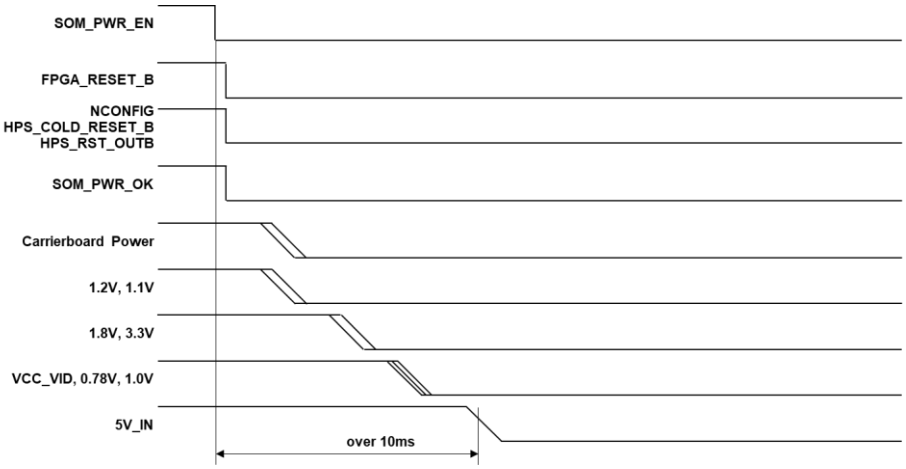


Figure 2-3 Power-Down Sequence

Important: Wait 10ms after setting SOM_PWR_EN low before dropping 5V_IN to follow the power-down sequence.

2.2. **Reset Circuit**

Figure 2-4 shows the Reset Circuit of this product. Reset control on the SoM is managed by the ADM1168. Additionally, three of reset factors can be input externally: Re-Configuration, HPS Cold Reset, and FPGA Reset.

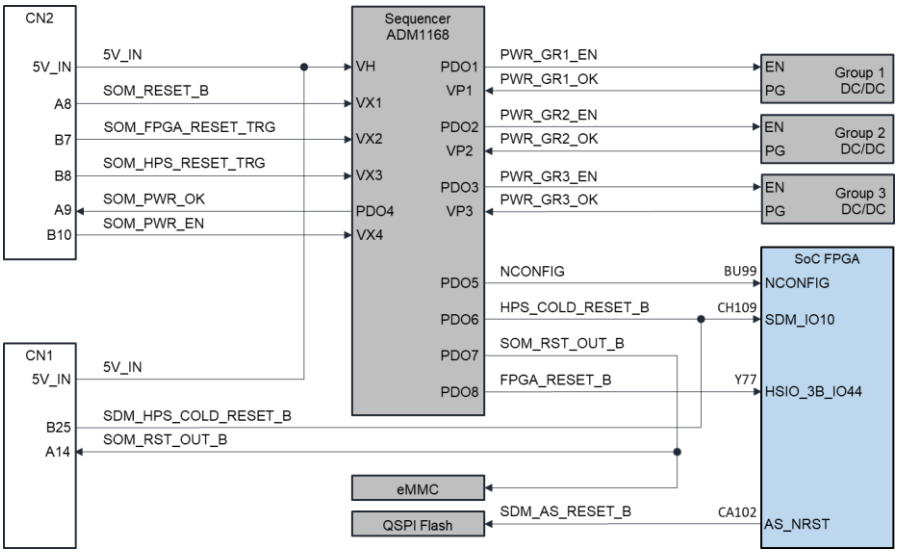


Figure 2-4 Reset Circuit

2.2.1. **Reset Timing: Re-Configuration**

Allow you to reconfiguration for this product by keeping the SOM_RESET_B signal low for 0.3ms or more.

Figure 2-5 shows the timing diagram.

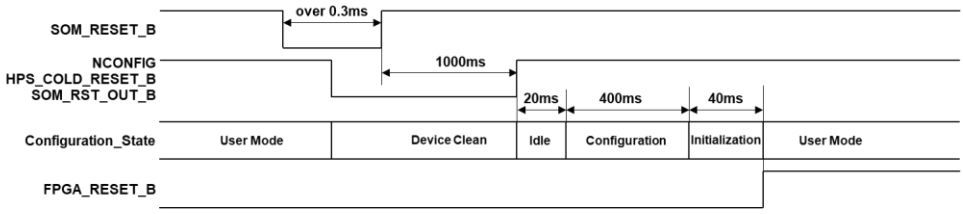


Figure 2-5 Re-Configuration Timing

2.2.2. **Reset Timing: HPS Cold Reset**

Allow you to reset for HPS on this product by keeping the SOM_HPS_RESET_TRG_B signal low for 0.3ms or more. Figure 2-6 shows the timing diagram.

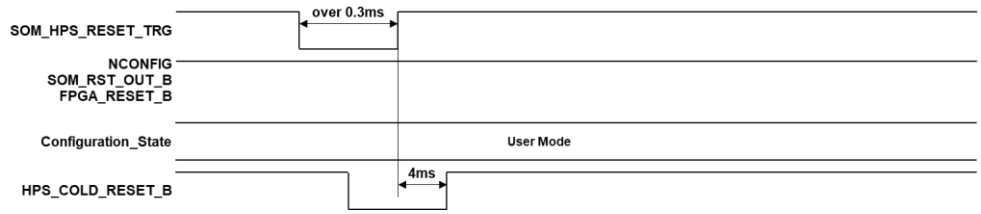


Figure 2-6 HPS Cold Reset Timing

2.2.3. **Reset Timing: FPGA Reset**

Allow you to reset for FPGA on this product by keeping the SOM_FPGA_RESET_TRG_B signal low for 0.3ms or more. Figure 2-7 shows the timing diagram.

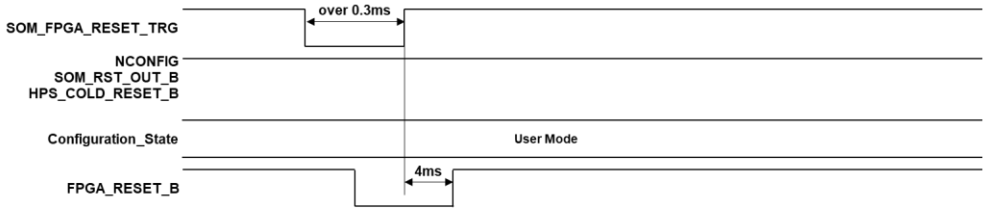


Figure 2-7 FPGA Reset Timing

2.3. **Clock Circuit**

Figure 2-8 shows the Clock Circuit of this product.

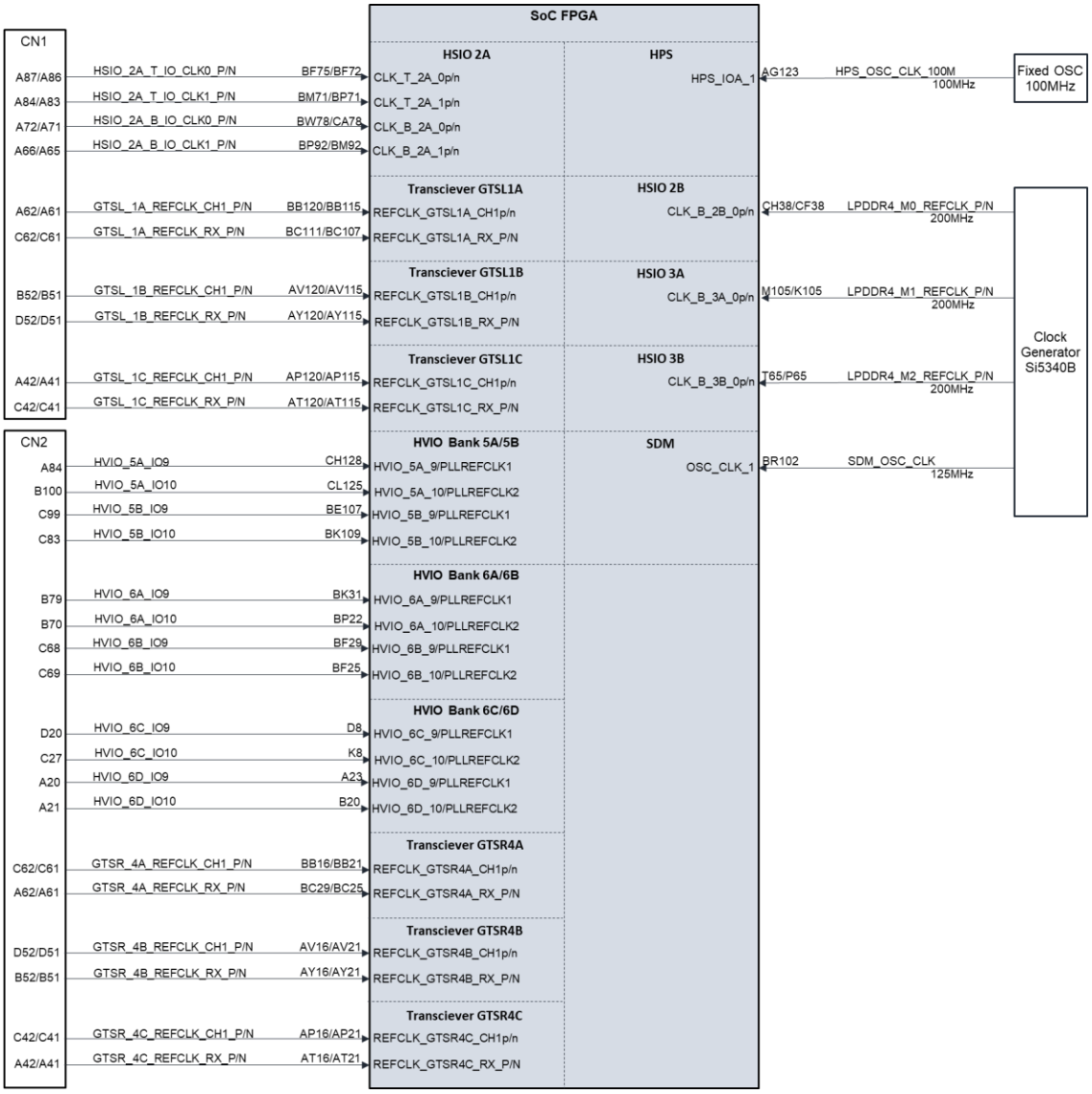


Figure 2-8 Clock Circuit

2.4. **SDMMC Interface**

This product is equipped with a microSD Card Slot and eMMC memory as storage memory. Storage memory selection is selected by SW1. Figure 2-9 shows the SDMMC Interface Circuit of this product, and Table 2-1 the specifications of SW1.

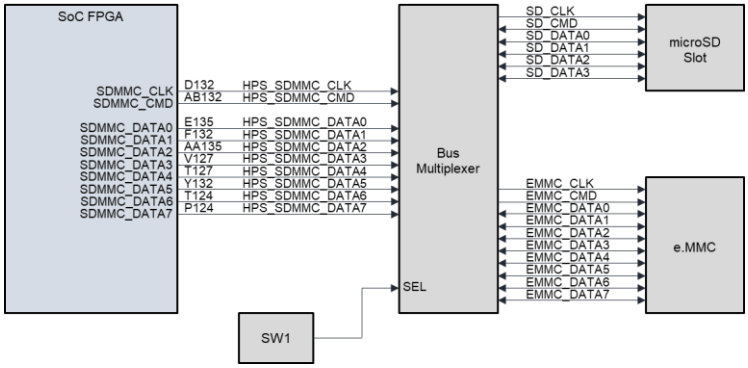


Figure 2-9 SDMMC Interface

2.5. **Configuration Circuit**

Figure 2-10 shows the Configuration Circuit of this product. The configuration source device can be set be SW1. Table 2-1 shows the relationship between the SW1 setting mode and the selected configuration source device.

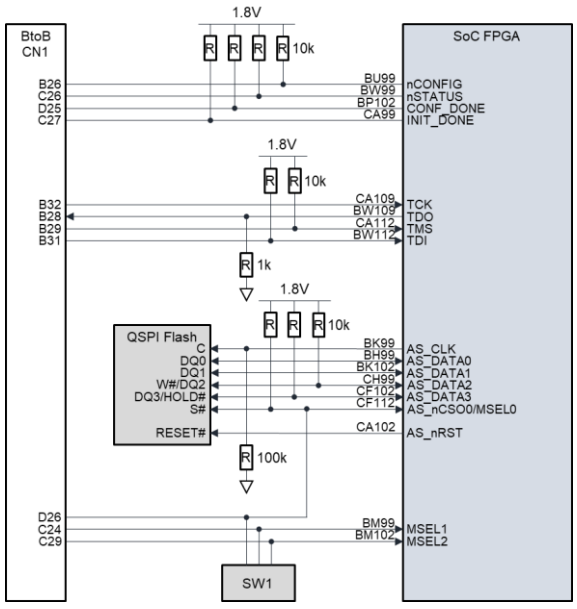
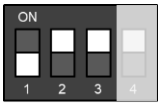


Figure 2-10 Configuration Circuit

2.6. **Mode Switch**

This product is equipped with a switch to set the operating mode. Table 2-1 shows the switch features.

Table 2-1 Mode Switch

<table>
<tr><th>Reference</th><th>Name</th><th>Description</th></tr>
<tr><td>SW1.1</td><td>MSEL0</td><td rowspan="3">Configuration Mode Selection
<table>
<tr><th>Mode</th><th>MSEL0</th><th>MSEL1</th><th>MSEL2</th><th>Drawing</th></tr>
<tr><td>JTAG only mode (Default)</td><td>OFF</td><td>OFF</td><td>OFF</td><td> 
</td></tr>
<tr><td>AS Normal mode</td><td>OFF</td><td>OFF</td><td>ON</td><td> 
</td></tr>
<tr><td>AS Fast mode</td><td>OFF</td><td>ON</td><td>ON</td><td> 
</td></tr>
</table></td></tr>
<tr><td>SW1.2</td><td>MSEL1</td></tr>
<tr><td>SW1.3</td><td>MSEL2</td></tr>
<tr><td>SW1.4</td><td>SDMMC_SEL</td><td>Storage Memory Selection
ON: SD mode (Default)
OFF: eMMC mode</td></tr>
</table>

Note: For more information on MSEL, please check the Agilex™ 5 FPGA & SoC E-Series manual.

2.7. **Status LED**

Table 2-2 shows the functions of the Status LED of this product.

Table 2-2 Status LED

Reference	Name	Description
LED1	CONF_DONE LED	Indicates configuration status. Turns On when configuration is complete.
LED2	User LED	General purpose LED for users. Turns On when HPS_IOA12 is set to Low and turns Off when set to High.
LED3	Power LED	Indicates power input status. Turns On when 5V power is applied.

2.8. BtoB Connector (CN1, CN2)

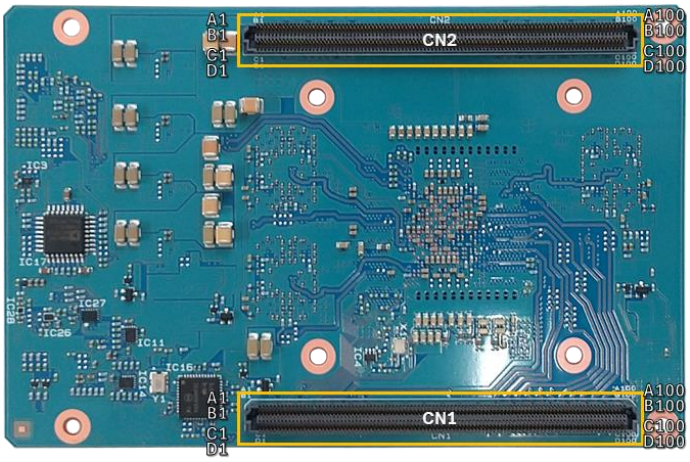


Figure 2-1 BtoB Connector Board Layout

2.8.1. CN1 Pin Assignments

Table 2-3 CN1 Pin Assignments

Pin No.	Row A	Row B	Row C	Row D
1	5V_IN	5V_IN	5V_IN	5V_IN
2	5V_IN	5V_IN	5V_IN	5V_IN
3	5V_IN	5V_IN	5V_IN	5V_IN
4	GND	5V_IN	GND	5V_IN
5	HPS_ULPI_DATA5	5V_IN	SOM_RSVD	5V_IN
6	HPS_ULPI_DATA3	GND	SOM_RSVD	GND
7	GND	HPS_ULPI_DATA2	GND	HPS_RGMII_TX_CLK
8	HPS_ULPI_DATA7	HPS_ULPI_DATA6	HPS_RGMII_RX_CLK	HPS_RGMII_TX_CTRL
9	HPS_ULPI_DATA1	GND	HPS_RGMII_RX_CTRL	GND
10	GND	HPS_ULPI_DATA4	GND	HPS_RGMII_TXD0
11	HPS_ULPI_DATA0	HPS_ULPI_CLK	HPS_RGMII_RXD0	HPS_RGMII_TXD1
12	HPS_ULPI_NXT	GND	HPS_RGMII_RXD1	GND
13	GND	HPS_ULPI_STP	GND	HPS_RGMII_TXD2
14	SOM_RST_OUT_B_1V8	HPS_ULPI_DIR	HPS_RGMII_RXD2	HPS_RGMII_TXD3
15	-	GND	HPS_RGMII_RXD3	GND
16	GND	HPS_INT_B_1V8	GND	HPS_ETH_MDIO
17	HPS_UART_TXD	HPS_IOB5_1V8	HPS_I2C_SCL_1V8	HPS_ETH_MDC
18	HPS_UART_RXD	GND	HPS_I2C_SDA_1V8	GND
19	GND	HPS_1PPS_OUT	GND	HPS_ETH_INT_B
20	HPS_IOB12_1V8	HPS_1PPS_IN	HPS_IOA12_1V8	-
21	HPS_IOB11_1V8	GND	HPS_IOA11_1V8	GND
22	GND	HPS_IOB10_1V8	GND	SOM_RSVD
23	-	HPS_IOB9_1V8	-	SOM_RSVD
24	-	GND	SDM_MSEL1_B2B_1V8	GND
25	GND	SDM_HPS_COLD_RESET_B_1V8	GND	SDM_CONF_DONE_1V8
26	SDM_TEMPDIODE0A_N	SDM_NCONFIG_1V8	SDM_NSTATUS_1V8	SDM_MSEL0_B2B_1V8
27	SDM_TEMPDIODE0A_P	GND	SDM_INIT_DONE_1V8	GND
28	GND	SOM_JTAG_TDO_1V8	GND	SDM_IO13_1V8
29	SOM_PMBUS_SDA_3V3	SOM_JTAG_TMS_1V8	SDM_MSEL2_B2B_1V8	SDM_IO12_1V8
30	SOM_PMBUS_SCL_3V3	GND	SOM_SDMMC_SEL_B2B_1V8	GND
31	GND	SOM_JTAG_TDI_1V8	GND	-
32	GND	SOM_JTAG_TCK_1V8	GND	SDM_IO8_1V8
33	GTSL_1C_TX_CH3_N	GND	GTSL_1C_TX_CH2_N	GND
34	GTSL_1C_TX_CH3_P	GND	GTSL_1C_TX_CH2_P	GND
35	GND	GTSL_1C_RX_CH3_N	GND	GTSL_1C_RX_CH2_N
36	GND	GTSL_1C_RX_CH3_P	GND	GTSL_1C_RX_CH2_P
37	GTSL_1C_TX_CH1_N	GND	GTSL_1C_TX_CH0_N	GND

Pin No.	Row A	Row B	Row C	Row D
38	GTSL_1C_TX_CH1_P	GND	GTSL_1C_TX_CH0_P	GND
39	GND	GTSL_1C_RX_CH1_N	GND	GTSL_1C_RX_CH0_N
40	GND	GTSL_1C_RX_CH1_P	GND	GTSL_1C_RX_CH0_P
41	GTSL_1C_REFCLK_CH1_N	GND	GTSL_1C_REFCLK_RX_N	GND
42	GTSL_1C_REFCLK_CH1_P	GND	GTSL_1C_REFCLK_RX_P	GND
43	GND	GTSL_1B_TX_CH3_N	GND	GTSL_1B_TX_CH2_N
44	GND	GTSL_1B_TX_CH3_P	GND	GTSL_1B_TX_CH2_P
45	GTSL_1B_RX_CH3_N	GND	GTSL_1B_RX_CH2_N	GND
46	GTSL_1B_RX_CH3_P	GND	GTSL_1B_RX_CH2_P	GND
47	GND	GTSL_1B_TX_CH1_N	GND	GTSL_1B_TX_CH0_N
48	GND	GTSL_1B_TX_CH1_P	GND	GTSL_1B_TX_CH0_P
49	GTSL_1B_RX_CH1_N	GND	GTSL_1B_RX_CH0_N	GND
50	GTSL_1B_RX_CH1_P	GND	GTSL_1B_RX_CH0_P	GND
51	GND	GTSL_1B_REFCLK_CH1_N	GND	GTSL_1B_REFCLK_RX_N
52	GND	GTSL_1B_REFCLK_CH1_P	GND	GTSL_1B_REFCLK_RX_P
53	GTSL_1A_TX_CH3_N	GND	GTSL_1A_TX_CH2_N	GND
54	GTSL_1A_TX_CH3_P	GND	GTSL_1A_TX_CH2_P	GND
55	GND	GTSL_1A_RX_CH3_N	GND	GTSL_1A_RX_CH2_N
56	GND	GTSL_1A_RX_CH3_P	GND	GTSL_1A_RX_CH2_P
57	GTSL_1A_TX_CH1_N	GND	GTSL_1A_TX_CH0_N	GND
58	GTSL_1A_TX_CH1_P	GND	GTSL_1A_TX_CH0_P	GND
59	GND	GTSL_1A_RX_CH1_N	GND	GTSL_1A_RX_CH0_N
60	GND	GTSL_1A_RX_CH1_P	GND	GTSL_1A_RX_CH0_P
61	GTSL_1A_REFCLK_CH1_N	GND	GTSL_1A_REFCLK_RX_N	GND
62	GTSL_1A_REFCLK_CH1_P	GND	GTSL_1A_REFCLK_RX_P	GND
63	GND	HSIO_2A_B_IO_N5	GND	HSIO_2A_B_IO_N17
64	GND	HSIO_2A_B_IO_P5	GND	HSIO_2A_B_IO_P17
65	HSIO_2A_B_IO_CLK1_N	GND	HSIO_2A_B_IO_N11	GND
66	HSIO_2A_B_IO_CLK1_P	HSIO_2A_B_IO_N4	HSIO_2A_B_IO_P11	HSIO_2A_B_IO_N18
67	GND	HSIO_2A_B_IO_P4	GND	HSIO_2A_B_IO_P18
68	HSIO_2A_B_IO_N1	GND	HSIO_2A_B_IO_N12	GND
69	HSIO_2A_B_IO_P1	HSIO_2A_B_IO_N3	HSIO_2A_B_IO_P12	HSIO_2A_B_IO_N16
70	GND	HSIO_2A_B_IO_P3	GND	HSIO_2A_B_IO_P16
71	HSIO_2A_B_IO_CLK0_N	GND	HSIO_2A_B_IO_N10	GND
72	HSIO_2A_B_IO_CLK0_P	HSIO_2A_B_IO_N2	HSIO_2A_B_IO_P10	HSIO_2A_B_IO_N15
73	GND	HSIO_2A_B_IO_P2	GND	HSIO_2A_B_IO_P15
74	HSIO_2A_B_IO_N23	GND	HSIO_2A_B_IO_N9	GND
75	HSIO_2A_B_IO_P23	HSIO_2A_B_IO_N24	HSIO_2A_B_IO_P9	HSIO_2A_B_IO_N14
76	GND	HSIO_2A_B_IO_P24	GND	HSIO_2A_B_IO_P14
77	HSIO_2A_B_IO_N22	GND	HSIO_2A_B_IO_N8	GND
78	HSIO_2A_B_IO_P22	HSIO_2A_B_IO_N21	HSIO_2A_B_IO_P8	HSIO_2A_B_IO_N13
79	GND	HSIO_2A_B_IO_P21	GND	HSIO_2A_B_IO_P13
80	HSIO_2A_B_IO_N20	GND	HSIO_2A_B_IO_N19	GND
81	HSIO_2A_B_IO_P20	HSIO_2A_T_IO_N17	HSIO_2A_B_IO_P19	HSIO_2A_B_VCCIO
82	GND	HSIO_2A_T_IO_P17	GND	HSIO_2A_B_VCCIO
83	HSIO_2A_T_IO_CLK1_N	GND	HSIO_2A_T_IO_N6	GND
84	HSIO_2A_T_IO_CLK1_P	HSIO_2A_T_IO_N16	HSIO_2A_T_IO_P6	HSIO_2A_T_IO_N11
85	GND	HSIO_2A_T_IO_P16	GND	HSIO_2A_T_IO_P11
86	HSIO_2A_T_IO_CLK0_N	GND	HSIO_2A_T_IO_N5	GND
87	HSIO_2A_T_IO_CLK0_P	HSIO_2A_T_IO_N15	HSIO_2A_T_IO_P5	HSIO_2A_T_IO_N12
88	GND	HSIO_2A_T_IO_P15	GND	HSIO_2A_T_IO_P12
89	HSIO_2A_T_IO_N21	GND	HSIO_2A_T_IO_N4	GND
90	HSIO_2A_T_IO_P21	HSIO_2A_T_IO_N14	HSIO_2A_T_IO_P4	HSIO_2A_T_IO_N10
91	GND	HSIO_2A_T_IO_P14	GND	HSIO_2A_T_IO_P10
92	HSIO_2A_T_IO_N20	GND	HSIO_2A_T_IO_N2	GND
93	HSIO_2A_T_IO_P20	HSIO_2A_T_IO_N13	HSIO_2A_T_IO_P2	HSIO_2A_T_IO_N9
94	GND	HSIO_2A_T_IO_P13	GND	HSIO_2A_T_IO_P9
95	HSIO_2A_T_IO_N24	GND	HSIO_2A_T_IO_N3	GND
96	HSIO_2A_T_IO_P24	HSIO_2A_T_IO_N1	HSIO_2A_T_IO_P3	HSIO_2A_T_IO_N8
97	GND	HSIO_2A_T_IO_P1	GND	HSIO_2A_T_IO_P8
98	HSIO_2A_T_IO_N23	GND	HSIO_2A_T_IO_N7	GND
99	HSIO_2A_T_IO_P23	HSIO_2A_T_IO_N22	HSIO_2A_T_IO_P7	HSIO_2A_T_VCCIO
100	GND	HSIO_2A_T_IO_P22	GND	HSIO_2A_T_VCCIO

2.8.2. **CN2 Pin Assignments**

Table 2-4 CN2 Pin Assignments

Pin No.	Row A	Row B	Row C	Row D
1	5V_IN	5V_IN	5V_IN	5V_IN
2	5V_IN	5V_IN	5V_IN	5V_IN
3	5V_IN	5V_IN	5V_IN	5V_IN
4	GND	5V_IN	GND	5V_IN
5	SOM_RSVD	5V_IN	SOM_RSVD	5V_IN
6	SOM_RSVD	GND	SOM_RSVD	GND
7	GND	SOM_FPGA_RESET_TRG_1V8	GND	SOM_RSVD
8	SOM_RESET_B_1V8	SOM_HPS_RESET_TRG_1V8	SOM_CLKG_SCL_1V8	SOM_RSVD
9	SOM_PWR_OK	GND	SOM_CLKG_SDA_1V8	GND
10	GND	SOM_PWR_EN	GND	1.8V_VCCBAT
11	HVIO_6D_VCCIO	-	-	-
12	HVIO_6D_VCCIO	GND	-	GND
13	GND	HVIO_6D_IO17	GND	HVIO_6C_IO3
14	HVIO_6D_IO18	HVIO_6D_IO20	HVIO_6C_IO2	HVIO_6C_IO1
15	HVIO_6D_IO19	GND	HVIO_6C_IO7	GND
16	GND	HVIO_6D_IO15	GND	HVIO_6C_IO4
17	HVIO_6D_IO14	HVIO_6D_IO16	HVIO_6C_IO6	HVIO_6C_IO5
18	HVIO_6D_IO13	GND	HVIO_6C_IO8	GND
19	GND	HVIO_6D_IO11	GND	HVIO_6C_IO11
20	HVIO_6D_IO9	HVIO_6D_IO12	HVIO_6C_IO14	HVIO_6C_IO9
21	HVIO_6D_IO10	GND	HVIO_6C_IO13	GND
22	GND	HVIO_6D_IO7	GND	HVIO_6C_IO15
23	HVIO_6D_IO6	HVIO_6D_IO8	HVIO_6C_IO19	HVIO_6C_IO17
24	HVIO_6D_IO5	GND	HVIO_6C_IO20	GND
25	GND	HVIO_6D_IO3	GND	HVIO_6C_IO16
26	HVIO_6D_IO1	HVIO_6D_IO4	HVIO_6C_IO12	HVIO_6C_IO18
27	HVIO_6D_IO2	GND	HVIO_6C_IO10	GND
28	GND	-	GND	HVIO_6C_VCCIO
29	-	-	-	HVIO_6C_VCCIO
30	-	GND	-	GND
31	GND	-	GND	-
32	GND	-	GND	-
33	GTSR_4C_RX_CH2_N	GND	GTSR_4C_RX_CH3_N	GND
34	GTSR_4C_RX_CH2_P	GND	GTSR_4C_RX_CH3_P	GND
35	GND	GTSR_4C_TX_CH2_N	GND	GTSR_4C_TX_CH3_N
36	GND	GTSR_4C_TX_CH2_P	GND	GTSR_4C_TX_CH3_P
37	GTSR_4C_RX_CH0_N	GND	GTSR_4C_RX_CH1_N	GND
38	GTSR_4C_RX_CH0_P	GND	GTSR_4C_RX_CH1_P	GND
39	GND	GTSR_4C_TX_CH0_N	GND	GTSR_4C_TX_CH1_N
40	GND	GTSR_4C_TX_CH0_P	GND	GTSR_4C_TX_CH1_P
41	GTSR_4C_REFCLK_RX_N	GND	GTSR_4C_REFCLK_CH1_N	GND
42	GTSR_4C_REFCLK_RX_P	GND	GTSR_4C_REFCLK_CH1_P	GND
43	GND	GTSR_4B_RX_CH2_N	GND	GTSR_4B_RX_CH3_N
44	GND	GTSR_4B_RX_CH2_P	GND	GTSR_4B_RX_CH3_P
45	GTSR_4B_TX_CH2_N	GND	GTSR_4B_TX_CH3_N	GND
46	GTSR_4B_TX_CH2_P	GND	GTSR_4B_TX_CH3_P	GND
47	GND	GTSR_4B_RX_CH0_N	GND	GTSR_4B_RX_CH1_N
48	GND	GTSR_4B_RX_CH0_P	GND	GTSR_4B_RX_CH1_P
49	GTSR_4B_TX_CH0_N	GND	GTSR_4B_TX_CH1_N	GND
50	GTSR_4B_TX_CH0_P	GND	GTSR_4B_TX_CH1_P	GND
51	GND	GTSR_4B_REFCLK_RX_N	GND	GTSR_4B_REFCLK_CH1_N
52	GND	GTSR_4B_REFCLK_RX_P	GND	GTSR_4B_REFCLK_CH1_P
53	GTSR_4A_RX_CH2_N	GND	GTSR_4A_RX_CH3_N	GND
54	GTSR_4A_RX_CH2_P	GND	GTSR_4A_RX_CH3_P	GND
55	GND	GTSR_4A_TX_CH2_N	GND	GTSR_4A_TX_CH3_N
56	GND	GTSR_4A_TX_CH2_P	GND	GTSR_4A_TX_CH3_P
57	GTSR_4A_RX_CH0_N	GND	GTSR_4A_RX_CH1_N	GND
58	GTSR_4A_RX_CH0_P	GND	GTSR_4A_RX_CH1_P	GND

Pin No.	Row A	Row B	Row C	Row D
59	GND	GTSR_4A_TX_CH0_N	GND	GTSR_4A_TX_CH1_N
60	GND	GTSR_4A_TX_CH0_P	GND	GTSR_4A_TX_CH1_P
61	GTSR_4A_REFCLK_RX_N	GND	GTSR_4A_REFCLK_CH1_N	GND
62	GTSR_4A_REFCLK_RX_P	GND	GTSR_4A_REFCLK_CH1_P	GND
63	GND	-	GND	-
64	GND	-	GND	-
65	HVIO_6A_IO19	GND	HVIO_6B_IO8	GND
66	HVIO_6A_IO15	HVIO_6A_IO17	HVIO_6B_IO4	HVIO_6B_IO3
67	GND	HVIO_6A_IO18	GND	HVIO_6B_IO5
68	HVIO_6A_IO13	GND	HVIO_6B_IO9	GND
69	HVIO_6A_IO12	HVIO_6A_IO20	HVIO_6B_IO10	HVIO_6B_IO6
70	GND	HVIO_6A_IO10	GND	HVIO_6B_IO7
71	HVIO_6A_IO1	GND	HVIO_6B_IO11	GND
72	HVIO_6A_IO7	HVIO_6A_IO14	HVIO_6B_IO1	HVIO_6B_IO2
73	GND	HVIO_6A_IO3	GND	HVIO_6B_IO13
74	HVIO_6A_IO6	GND	HVIO_6B_IO12	GND
75	HVIO_6A_IO2	HVIO_6A_IO16	HVIO_6B_IO15	HVIO_6B_IO16
76	GND	HVIO_6A_IO11	GND	HVIO_6B_IO14
77	HVIO_6A_IO5	GND	HVIO_6B_IO18	GND
78	HVIO_6A_IO8	HVIO_6A_IO4	HVIO_6B_IO17	HVIO_6B_IO20
79	GND	HVIO_6A_IO9	GND	HVIO_6B_IO19
80	HVIO_6A_VCCIO	GND	-	GND
81	HVIO_6A_VCCIO	HVIO_5A_IO13	-	HVIO_6B_VCCIO
82	GND	HVIO_5A_IO14	GND	HVIO_6B_VCCIO
83	HVIO_5A_IO7	GND	HVIO_5B_IO10	GND
84	HVIO_5A_IO9	HVIO_5A_IO11	HVIO_5B_IO8	HVIO_5B_IO6
85	GND	HVIO_5A_IO16	GND	HVIO_5B_IO16
86	HVIO_5A_IO12	GND	HVIO_5B_IO13	GND
87	HVIO_5A_IO2	HVIO_5A_IO1	HVIO_5B_IO7	HVIO_5B_IO2
88	GND	HVIO_5A_IO15	GND	HVIO_5B_IO12
89	HVIO_5A_VCCIO	GND	HVIO_5B_IO18	GND
90	HVIO_5A_VCCIO	-	HVIO_5B_IO17	HVIO_5B_VCCIO
91	GND	-	GND	HVIO_5B_VCCIO
92	HVIO_5A_IO4	GND	HVIO_5B_IO5	GND
93	HVIO_5A_IO18	HVIO_5A_IO8	HVIO_5B_IO15	HVIO_5B_IO14
94	GND	HVIO_5A_IO3	GND	HVIO_5B_IO19
95	HVIO_5A_IO5	GND	HVIO_5B_IO4	GND
96	HVIO_5A_IO17	HVIO_5A_IO6	HVIO_5B_IO20	HVIO_5B_IO1
97	GND	HVIO_5A_IO20	GND	HVIO_5B_IO3
98	SOM_RSVD	GND	HVIO_5B_IO11	GND
99	SOM_RSVD	HVIO_5A_IO19	HVIO_5B_IO9	SOM_RSVD
100	GND	HVIO_5A_IO10	GND	SOM_RSVD

2.8.3. **Signal Names and Descriptions**

Table 2-5 Signal Names and Descriptions

Signal Name	Dir	Voltage	Connect	Description
5V_IN	In	5V	Power Circuit	SoM power input
GND	-	-	GND	Ground
1.8V_VCCBAT	In	1.8V	VCCBAT	Battery backup power input for AES
SOM_RSVD	-	-	Not Connect	Reserved pin.
HPS_ULPI_DATA[7:0]	I/O	1.8V	HPS	USB ULPI data bus
HPS_ULPI_CLK	In	1.8V	HPS	USB ULPI clock
HPS_ULPI_NXT	In	1.8V	HPS	USB ULPI NXT signal
HPS_ULPI_STP	Out	1.8V	HPS	USB ULPI STP signal
HPS_ULPI_DIR	In	1.8V	HPS	USB ULPI DIR signal
HPS_RGMII_TX_CLK	Out	1.8V	HPS	Ethernet RGMII transmit clock
HPS_RGMII_TX_CTRL	Out	1.8V	HPS	Ethernet RGMII transmit control
HPS_RGMII_TXD[3:0]	Out	1.8V	HPS	Ethernet RGMII transmit data
HPS_RGMII_RX_CLK	In	1.8V	HPS	Ethernet RGMII receive clock
HPS_RGMII_RX_CTRL	In	1.8V	HPS	Ethernet RGMII receive control
HPS_RGMII_RXD[3:0]	In	1.8V	HPS	Ethernet RGMII receive data
HPS_ETH_MDIO	I/O	1.8V	HPS	Ethernet PHY management data
HPS_ETH_MDC	Out	1.8V	HPS	Ethernet PHY management clock

Signal Name	Dir	Voltage	Connect	Description
HPS_ETH_INT_B	In	1.8V	HPS	Ethernet PHY interrupt signal
SOM_RST_OUT_B_1V8	Out	1.8V	Reset Circuit	Reset output
HPS_UART_TXD	Out	1.8V	HPS	UART transmit data
HPS_UART_RXD	In	1.8V	HPS	UART receive data
HPS_I2C_SCL_1V8	Out	1.8V	HPS	I2C clock
HPS_I2C_SDA_1V8	I/O	1.8V	HPS	I2C data
HPS_IOA[n]_1V8	I/O	1.8V	HPS	HPS IO port A: n is a number
HPS_IOB[n]_1V8	I/O	1.8V	HPS	HPS IO port B: n is a number
SDM_TEMPDIODE0A_[P/N]	In	1.8V	SDM	Diode input for temperature detection
SDM_MSEL[2:0]_B2B_1V8	In	1.8V	SDM	FPGA MSEL signal
SDM_NSTATUS_1V8	Out	1.8V	SDM	FPGA NSTATUS signal
SDM_CONF_DONE_1V8	Out	1.8V	SDM	FPGA CONF_DONE signal
SDM_INIT_DONE_1V8	Out	1.8V	SDM	FPGA INIT_DONE signal
SDM_IO[n]	I/O	1.8V	SDM	SDM IO port: n is a number
SOM_PMBUS_SDA_3V3	I/O	3.3V	Power Circuit	PMBus data
SOM_PMBUS_SCL_3V3	In	3.3V	Power Circuit	PMBus clock
SOM_CLKG_SCL_1V8	In	1.8V	Clock Circuit	I2C clock (Clock Generator)
SOM_CLKG_SDA_1V8	In	1.8V	Clock Circuit	I2C data (Clock Generator)
SOM_RESET_B_1V8	In	1.8V	Power Circuit	Re-Configuration request
SOM_FPGA_RESET_TRG_1V8	In	1.8V	Power Circuit	FPGA Reset request
SOM_HPS_RESET_TRG_1V8	In	1.8V	Power Circuit	HPS Cold Reset request
SOM_PWR_OK	Out	1.8V	Power Circuit	SOM Power OK signal
SOM_PWR_EN	In	1.8V	Power Circuit	SOM Power Enable signal
GTS[L/R]_[1/4][A/B/C]_TX_CH[3:0]_[P/N]	Out	1.0V	Transceiver	GTS Transceiver transmit data
GTS[L/R]_[1/4][A/B/C]_RX_CH[3:0]_[P/N]	In	1.0V	Transceiver	GTS Transceiver receive data
GTS[L/R]_[1/4][A/B/C]_REFCLK_RX_[P/N]	In	1.0V	Transceiver	GTS Transceiver regional reference clock
GTS[L/R]_[1/4][A/B/C]_REFCLK_CH1_[P/N]	In	1.0V	Transceiver	GTS Transceiver local reference clock
HSIO_2A_B_VCCIO	In	1.0V - 1.3V	Bank 2AB	VCCIO (Bank 2AB) voltage input
HSIO_2A_B_IO_[P/N][n]	I/O	HSIO_2A_B_VCCIO	Bank 2AB	HSIO (Bank 2AB) port: n is a number
HSIO_2A_B_IO_CLK[n]_[P/N]	I/O	HSIO_2A_B_VCCIO	Bank 2AB	HSIO (Bank 2AB) port / clock input: n is a number
HSIO_2A_T_VCCIO	In	1.0V - 1.3V	Bank 2AT	VCCIO (Bank 2AT) voltage input
HSIO_2A_T_IO_[P/N][n]	I/O	HSIO_2A_T_VCCIO	Bank 2AT	HSIO port (Bank 2AT): n is a number
HSIO_2A_T_IO_CLK[n]_[P/N]	I/O	HSIO_2A_T_VCCIO	Bank 2AT	HSIO port (Bank 2AT) / clock input: n is a number
HVIO_5A_VCCIO	In	1.8V - 3.3V	Bank 5A	VCCIO (Bank 5A) voltage input
HVIO_5A_IO[n]	I/O	HVIO_5A_VCCIO	Bank 5A	HVIO (Bank 5A) port: n is a number
HVIO_6A_VCCIO	In	1.8V - 3.3V	Bank 6A	VCCIO (Bank 6A) voltage input
HVIO_6A_IO[n]	I/O	HVIO_6A_VCCIO	Bank 6A	HVIO (Bank6A) port: n is a number
HVIO_6B_VCCIO	In	1.8V - 3.3V	Bank 6B	VCCIO (Bank 6B) voltage input
HVIO_6B_IO[n]	I/O	HVIO_6B_VCCIO	Bank 6B	HVIO (Bank 6B) port: n is a number
HVIO_6C_VCCIO	In	1.8V - 3.3V	Bank 6C	VCCIO (Bank 6C) voltage input
HVIO_6C_IO[n]	I/O	HVIO_6D_VCCIO	Bank 6C	HVIO (Bank 6B) port: n is a number
HVIO_6D_VCCIO	In	1.8V - 3.3V	Bank 6D	VCCIO (Bank 6D) voltage input
HVIO_6D_IO[n]	I/O	HVIO_6D_VCCIO	Bank 6D	HVIO (Bank 6D) port: n is a number

3. Electrical Specifications

3.1. Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Power-supply voltage	VIN	-0.3	5.5	V	5V_IN
VCCIO voltage	VHSIO	-0.5	1.74	V	Bank_2A_T_VCCIO Bank_2A_B_VCCIO
	VHVIO	-0.5	3.74	V	HVIO_5A_VCCIO HVIO_5B_VCCIO HVIO_6A_VCCIO HVIO_6C_VCCIO HVIO_6D_VCCIO
VCCBAT voltage	VCCBAT	-0.5	2.08	V	1.8_VCCBAT
Input voltage	VI_HPS	-0.3	2.38	V	HPS
	VI_SDM	-0.3	2.38	V	SDM
	VI_HSIO	-0.3	VHSIO+0.25	V	HSIO
	VI_HVIO	-0.3	VHVIO+0.3	V	HVIO
	VI_18	-0.3	2.38	V	Signals with suffix _1V8 except for the above
	VI_33	-0.3	5.5	V	SOM_PMBUS_SCL_3V3 SOM_PMBUS_SDA_3V3
Operating temperature	Topr	-25	85	°C	No condensation

3.2. Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power-supply voltage	VIN	4.75	5.0	5.25	V	5V_IN
HSIO VCCIO voltage	VHSIO	1.261	1.3	1.339	V	Bank_2A_T_VCCIO
		1.164	1.2	1.236	V	Bank_2A_B_VCCIO
HVIO VCCIO voltage	VHVIO	3.201	3.3	3.399	V	HVIO_5A_VCCIO
		2.425	2.5	2.575	V	HVIO_5B_VCCIO
		1.746	1.8	1.854	V	HVIO_6A_VCCIO HVIO_6C_VCCIO HVIO_6D_VCCIO
VCCBAT voltage	VCCBAT	1	1 - 1.8	1.8	V	1.8_VCCBAT
Input voltage	HPS_VI	-0.3	1.8	2.1	V	HPS
	SDM_VI	-0.3	1.8	2.1	V	SDM
	HSIO_VI	-0.3		VHSIO+0.25	V	HSIO
	HVIO_VI	-0.3		VHVIO+0.3	V	HVIO
	VI_18	-0.3	1.8	2.1	V	Signals with suffix _1V8 except for the above
	VI_33	-0.3	3.3	3.6	V	SOM_PMBUS_SCL_3V3 SOM_PMBUS_SDA_3V3

3.3. IO Pin Specifications

IO Pin Specifications vary depending on bank voltage and settings. Please refer the latest Agilex™ 5 FPGA & SoC E-Series Datasheet for more details.

4. SoM Dimensions

Figure 3-1 shows the Dimensions of this product. (Unit: mm)

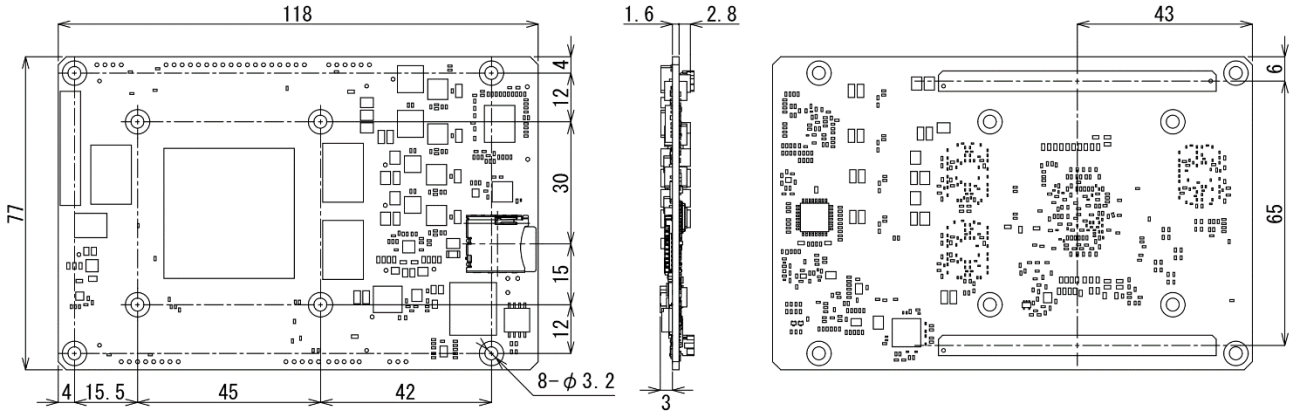


Figure 3-1 SoM Dimensions

5. Document History

Ver.	Date	Changes
1.0	2024/4/18	Initial release.