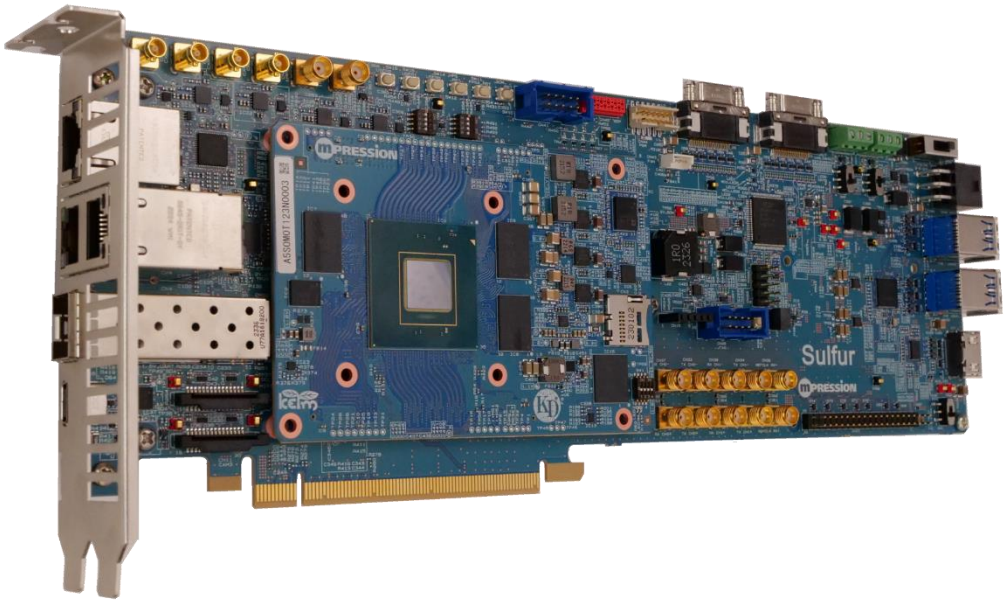
Sulfur Type-A Kit
User Manual

Ver.1.0



Kondo Electronics Industry Co., Ltd.

Introduction

Thank you for purchasing a Sulfur Type-A Kit.

Read this manual and related document thoroughly before using this product and observe the precautions for use.

CAUTION

- The contents of this manual are subject to change without prior notice. Contact the Kondo Electronics Industry service center or check the Kondo Electronics Industry website for the latest information before using the product.
- This product contains general electronic components. Do not use the product for devices that require extremely high reliability (aerospace equipment, nuclear power equipment, medical equipment for life support, etc.).
- This product is developed and manufactured for use only in Japan. If this product or a product that incorporates this product is exported outside Japan, all the necessary procedures must be completed at the responsibility and expense of the customer in accordance with the Foreign Exchange and Foreign Trade Act and other export laws and regulations.
- Be sure to turn off the power before inserting or removing cables to connectors other than LAN and USB.
- Do not use this product in locations subject to large amounts of water, humidity, dust, or oil smoke.
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Contact Information

- For any questions about this product, contact the following email address:

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1. Overview

This is the user manual that describes the features and specifications of the development kit “Sulfur Type-A Kit” equipped with Agilex™ 5 FPGA & SoC E-Series.

1.1. Product Features

This product is a kit that System on Module (referred to as SoM) KEIm-A5ESoM (Kondo Electronics Industries) equipped with Agilex™5 FPGA & SoC E-Series. The carrier board is equipped with peripheral interfaces such as MIPI, Camera Link, CoaXPress, 10GbE, Ethernet, USB3.1/2.0, and HDMI output. It is a platform that allows hardware and software developers to immediately evaluate using Agilex™5 FPGA & SoC E-Series. This product has the following features:

A) Already circuit is designed and evaluated
If you use this kit to evaluate devices and functions and then use the SoM as is for product design, allows you to shorten the development period.

B) PCIe Form Factor
Since it is in the form of a PCIe card, when developing applications using the PCIe interface, allows you to evaluate while installed on your PC.

C) Rich Peripherals
Equipped with various peripheral interfaces to evaluate more applications.

D) Various Reference Designs
Software is also required to operate the kit’s peripherals. This kit is planned to provide a variety of reference designs.

1.2. **Product Specifications**

Table 1-1 shows the product specifications of this product.

Table 1-1 Product Specifications

Item		Description
SoM		KEIm-A5ESoM (ES Version)
	SoC FPGA	A5ED065BB32AE5SR0 Processor: Dual-core Arm Cortex-A76, Dual-core Arm Cortex-A55 Logic Elements: 656 kLEs / 222,400 ALMs
	LPDDR4 SDRAM	4GByte (1G x 32bit) x3
	QSPI Flash	256MByte (2Gbit)
	eMMC	32GByte
	SD	microSD Card Slot
Ethernet (HPS)		Gigabit Ethernet Port x1 PHY: 88E1512-A0-NNP2 (Marvell)
Ethernet (FPGA)		Gigabit Ethernet Port x2 PHY: KSZ9131RNX (Microchip)
USB3.1 / 2.0		USB 3.1 Type-A (Host) Connector x4 USB 3.1 Gen1 (5Gbps) / USB2.0 Important: ES Version not support USB3.1 USB 3.1 Hub: TUSB8041 (TI) USB 2.0 PHY: USB3320C-EZK (Microchip)
10GbE		SFP+ Connector x1
HDMI Output		HDMI 2.0 Type-A Connector x1 HDMI 2.0 Redriver: TDP0604 (TI)
MIPI		15-pin Connector x2
		22-pin Connector x2
Camera Link		26-pin SDR Connector x2
SLVS-EC		8-lanes port x1
CoaXPress 2.0		CXP-12 (12Gbps) micro BNC x4 Transmitter / Receiver: EQCO125X40 (Microchip)
PCIe		PCIe Card Edge Connector PCIe Gen 4 x4
Clock		Crystal Oscillator Si564 (Skyworks) x3 Reference Clock for HDMI: 564BAAC001704CCG (Skyworks) Reference Clock for SLVS-EC: 564BAED002453CCG (Skyworks) Reference Clock for 10GbE: 564BAAC000771CCG (Skyworks)
		Clock Generator Si5340B-D-GM (Skyworks) 4-Outputs, Reference Clock for CXP, USB3.1, HSIO and HVIO
CAN		3 Terminal Block Connector x2 CAN Driver: TJA1057 (NXP) MCU for Protocol: LPC54616J512BD100 (NXP)
USB-UART		USB Type-C Connector x1 USB to UART Bridge: FT232RN (FTDI)
RTC		DS1339A (ADI), Battery backup
EEPROM		24AA64 (Microchip)
Debug I/F	SoC FPGA	JTAG 10-pin Connector
	MCU	SWD 10-pin Connector
	Clock Generator	CBPROG 10-pin Connector
	Power Sequencer	SDP 10-pin Connector
	SoM Power	PSM 10-pin Connector
Power Supply		+12V±10% (10.8V～13.2V) Input from ATX 6-pin Connector or PCIe Card Edge or both
Power Consumption		TBD
Operating Temperature		0°C~ +40°C
Dimensions		308.5×132.51x58.25mm (Protrusions not included)

1.3. **Block Diagram**

Figure 1-1 shows the block diagram of this product.

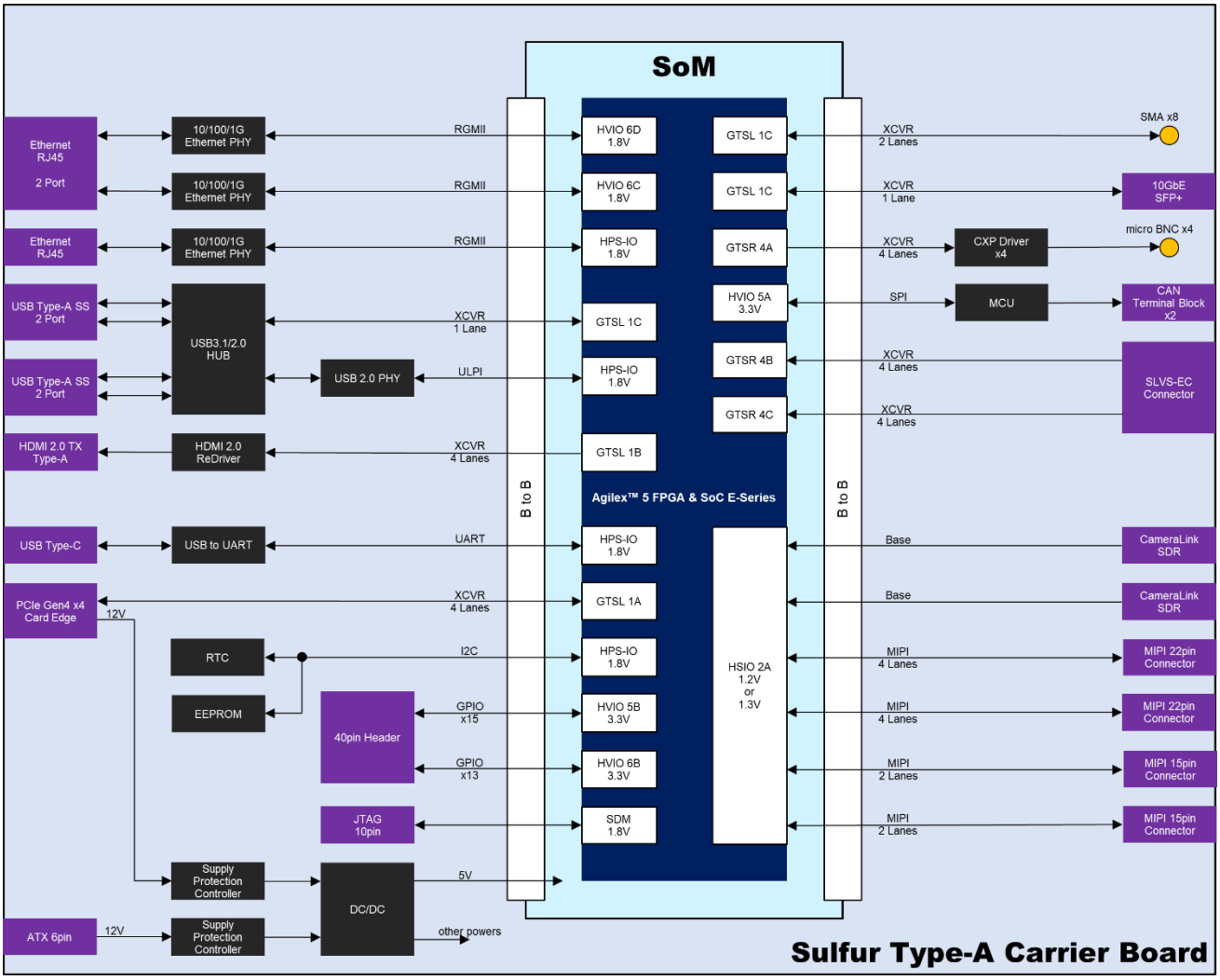


Figure 1-1 Sulfur Type-A Kit Brock Diagram

1.4. **Board Layout**

Figure 1-2, Figure 1-3 show the Board Layout of this product, and Table 1-2 lists the Major Components installed on this product.

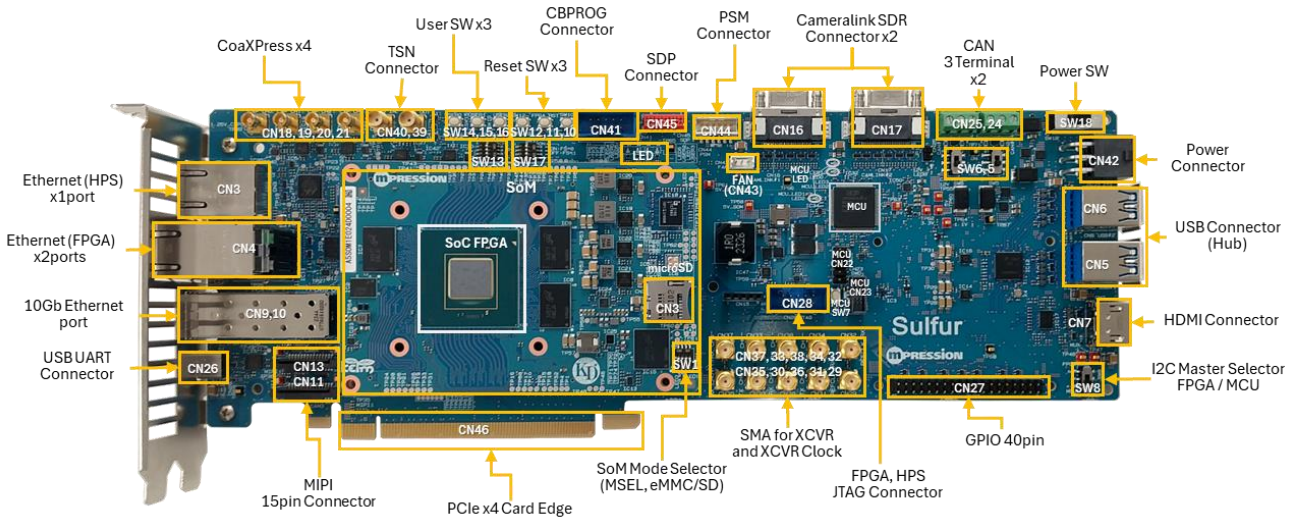


Figure 1-2 Board Top Side Layout

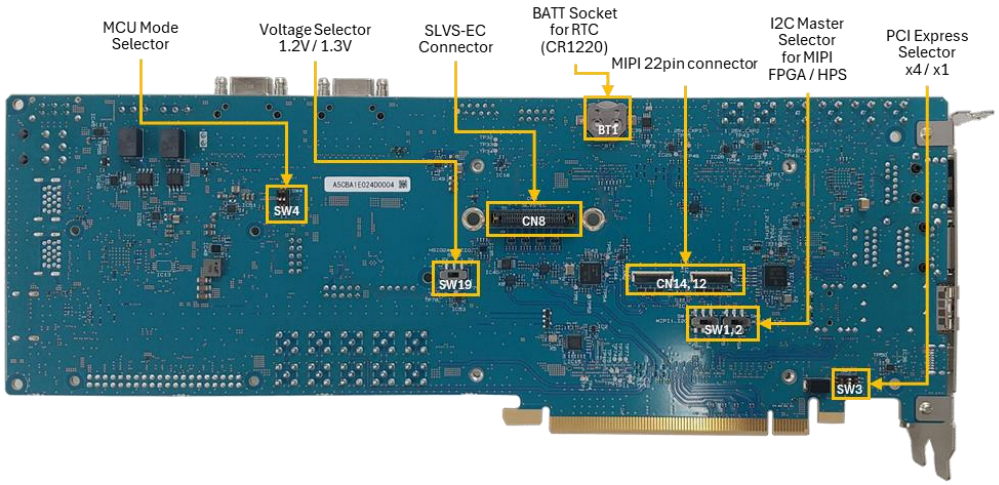


Figure 1-3 Board Bottom Side Layout

Table 1-2 List of Major Components

Reference	Name	Description
SoM KEIm-A5ESoM (Kondo Electronics Industry)		
SoM: IC1	SoC FPGA	Agilex™ 5 FPGA & SoC E-Serise A5ED065BB32AE5SR0
SoM: CN1, CN2	SoM Connector	400-pin BtoB Connector, 0.635 mm pitch, 4-Row Carrier Board Side: ADM6-100-01.5-L-4-2-A (Samtec) SoM Side: ADF6-100-03.5-L-4-2-A (Samtec)
SoM: CN3	microSD Card Slot	Connected to SDMMC of HPS
SoM: SW1	SoM Mode Switch	Used to set FPGA Configuration Mode and select Storage Memory
Gigabit Ethernet		
CN3	Ethernet (HPS) Port	RJ45 Connector with Magnetics
CN4	Ethernet (FPGA) Port	RJ45 Connector with Magnetics x2
10GbE		
CN9, CN10	10GbE port	SFP+ 20-pin Connector, Cage for SFP+
USB 3.1 / 2.0		
CN5, CN6	USB 3.1 Connector	USB 3.1 Type-A Connector x2
HDMI		
CN7	HDMI 2.0 Connector	HDMI 2.0 Type-A Connector
SLVS-EC		
CN8	SLVS-EC Connector	50-pin BtoB Connector, 0.8mm pitch, 2-Row ERM8-025-05.0-L-DV-L-K (Samtec)
MIPI		
CN11, CN13	MIPI 2-lane port	15-pin FFC Connector, 1 mm pitch
CN12, CN14	MIPI 4-lane port	22-pin FFC Connector, 0.5 mm pitch
SW1, SW2	MIPI I2C Master Selection Switch	FPGA / HPS Selection
PCIe		
CN46	PCIe Card Edge	x4 connection (physical shape is x16)
Camera Link		
CN16, CN17	Camera Link Connector	26-pin SDR Connector Each connector has a pin assignment for Base Configuration, and by using both connectors allows pin assignment for Full Configuration.
CoaXPress		
CN18, CN19, CN20, CN21	CoaXPress Connector	Micro BNC
CAN / MCU		
CN24, CN25	CAN Connector	3-Terminal Block Connector
SW5, SW6	CAN Termination Switch	Slide Switch, Controls termination ON/OFF
IC32	MCU	LPC54616J512BD100 (NXP) CAN Protocol Stack already implemented.
SW4	Mode Switch for MCU	Used to set MCU boot mode
SW8	MCU I2C Master Selection Switch	FPGA / MCU Selection
CN22	Pin-Header for MCU	2.54 mm pitch, 10-pin Header
LED1, LED2, LED3	Status LED for MCU	LED for checking MCU operation
USB-UART		
CN26	USB-UART Connector	USB Type-C
Battery		
BT1	Battery Holder	Battery backup for RTC (CR1220)
40-pin Header		
CN27	Pin Header	2.54 mm pitch, 40-pin Header, connected to 28-pin HVIO
Switch, LED		
SW10	Re-Configuration Switch	For FPGA Reconfiguration
SW11	FPGA Reset Switch	For FPGA Reset
SW12	HPS Cold Reset Switch	For HPS Reset
SW13	User DIP Switches	The switch has 4-elements, 3-elements of which are connected to HVIO.
SW14, SW15, SW16	User Push Switches	All switches connected to HVIO.
SW17	Clock Frequency Selection	Selection of Reference Clock Frequency for SLVS-EC

Reference	Name	Description
	Switch	
SW19	HSIO_2A Voltage Selection Switch	Bank 2A (HSIO) VCCIO Selection (1.2V or 1.3V)
LED4, LED5, LED6, LED7	User LEDs	All LEDs connected to HVIO.
SMA		
CN29, CN32	GTS Clock Input Connector	Connected to transceiver reference clock input.
CN30, CN33	GTS Tx channel Connector 0	Connected to transceiver transmit channel.
CN35, CN37	GTS Rx channel Connector 0	Connected to transceiver receiver channel.
CN31, CN34	GTS Tx channel Connector 1	Connected to transceiver transmit channel.
CN36, CN38	GTS Rx channel Connector 1	Connected to transceiver receiver channel.
CN39, CN40	TSN Synchronization signal Output / Input	Connected to PPS output and PPS input of HPS.
Debug I/F		
CN23	SWD Connector for MCU	1.27 mm pitch, 10-pin Header
CN28	JTAG Connector	10-pin, 2.54 mm pitch Allows you to debug or configuration of Agilex™5 FPGA & SoC E-Series by connecting Intel® FPGA Download Calbe II.
CN41	CBPROG Connector	Allows you to interface the Clock Generator Si5340 by connect CBPROG-DONGLE (Skyworks).
CN44	PSM Connector	Allows you to interface the Power Controller LTC7883 by connect DC1613A (ADI).
CN45	SDP Connector	Allows you to interface the Power Sequencer ADM1168 by connect USB-SDP-CABLEZZ (ADI).
Power Supply		
CN42	Power Input Connector	6-pin ATX, +12V input
SW18	Power Switch	Turn On / Off +12V supply to the Carrier Board.
CN43	FAN Connector	+12V output

2. Functional Specifications

This section describes the details of the various function implemented on this product.

2.1. SoM (KEIm-A5ESoM)

Table 2-1 shows the specifications of the SoM (KEIm-A5ESoM) installed int this product. For details, please refer to the KEIm-A5ESoM Hardware Manual.

Table 2-1 SoM Specifications

Item		Description
SoC FPGA		Agilex™ 5 FPGA & SoC E-Series
	Device	A5ED065BB32AE5SR0
	Processor	Dual-core Arm Cortex-A76, Dual-core Arm Cortex-A55
	Logic Elements / Adaptive logic modules	656 kLEs / 222,400 ALMs
	M20K memory blocks / size	1,611 blocks / 31.46 Mbits
	MLAB memory count / size	8,440 count / 6.79 Mbits
	I/O PLL	8
	Fabric-feeding I/O PLL	13
	Variable-precision DSP blocks	846
	18 x 19 multipliers	1,692
LPDDR4 SDRAM		4GByte (1G x 32bit) x3 MT53E1G32D2FW-046 (Micron)
QSPI Flash		256MByte (2Gbit) MT25QU02GCBB (Micron)
eMMC		32GByte MTFC32GAZAQHD (Micron)
SD		microSD Card Slot
Clock	OSC	100MHz
	Clock Generator	Low-Jitter 4-Output Clock Generator Si5340B-D-GM (Skyworks)
BtoB Connector		400-pin BtoB Connector x2
	Connector	ADF6-100-03.5-L-4-2-A (Samtec)
	HPS-IO	Ethernet (RGMII) x1, USB OTG (ULPI) x1, UART x1, I2C x1, QSPI x1, GPIO up to 21 (Depends on HPS configuration)
	HSIO	Up to 96-ports
	HVIO	Up to 120-ports
	Transceiver (17 Gbps)	24-lanes
	Debug I/F	JTAG
Power supply		+5V±5% (4.75V～5.25V), VCCIO (Depends on configuration)
Power consumption		TBD
Operating temperature		-25°C~ +85°C
Dimensions		118×77mm

2.1.1. **Configuration Circuit**

Figure 2-1 shows the SoM Configuration Circuit installed on this product. This product allows you to select the configuration source device by setting SW1. Table 2-2 shows the SW1 setting mode and the selected configuration device.

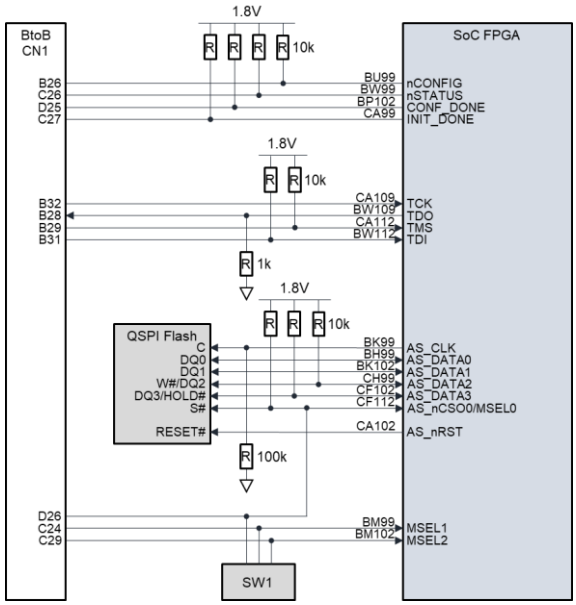
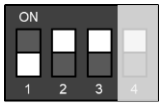


Figure 2-1 Configuration Circuit

2.1.2. **SoM Mode Switch**

Table 2-2 shows the functions of the Mode Switch implemented on the SoM of this product.

Table 2-2 SoM Mode Switch

<table>
<tr><th>Reference</th><th>Name</th><th>Description</th></tr>
<tr><td>SoM: SW1.1</td><td>MSEL0</td><td rowspan="3">Configuration Mode Selection
<table>
<tr><th>Mode</th><th>MSEL0</th><th>MSEL1</th><th>MSEL2</th><th>Drawing</th></tr>
<tr><td>JTAG only mode (Default)</td><td>OFF</td><td>OFF</td><td>OFF</td><td> 
</td></tr>
<tr><td>AS Normal mode</td><td>OFF</td><td>OFF</td><td>ON</td><td> 
</td></tr>
<tr><td>AS Fast mode</td><td>OFF</td><td>ON</td><td>ON</td><td> 
</td></tr>
</table></td></tr>
<tr><td>SoM: SW1.2</td><td>MSEL1</td><td></td></tr>
<tr><td>SoM: SW1.3</td><td>MSEL2</td><td></td></tr>
<tr><td>SoM: SW1.4</td><td>SDMMC_SEL</td><td>Storage Memory Selection
ON: SD mode (Default)
OFF: eMMC mode</td></tr>
</table>

Note: For more information on MSEL, please refer to the Agilex™ 5 FPGA & SoC E-Series manual.

2.1.3. **SoM Status LEDs**

Table 2-3 shows the functions of the Status LED implemented on the SoM of this product.

Table 2-3 SoM Status LEDs

Reference	Name	Description
SoM: LED1	CONF_DONE LED	Indicates configuration status. Turns On when configuration is complete.
SoM: LED2	USER LED	General purpose LED for users. Turns On when HPS_IOA12 is set to Low and turns Off when set to High.
SoM: LED3	POWER LED	Indicates power input status. Turns On when 5V power is applied.

2.2. **Power Circuit**

Figure 2-2 shows the Power Circuit of this product.

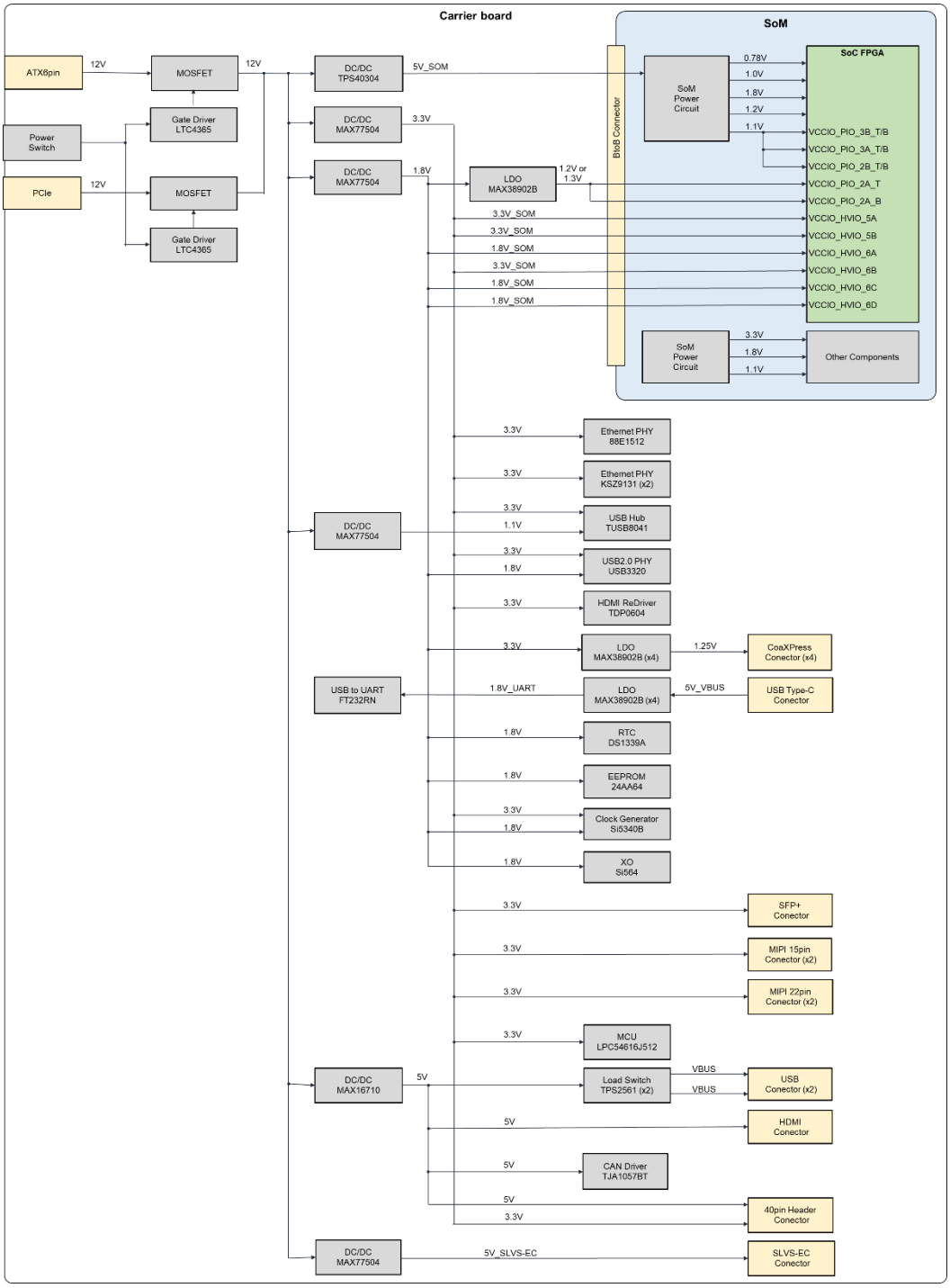


Figure 2-2 Power Circuit

2.3. **Reset Circuit**

Figure 2-4 shows the Reset Circuit of this product. Reset control is managed by ADM1168 implemented on the SoM. Additionally, three of reset factors allows you to input externally: Re-Configuration, HPS Cold Reset, and FPGA Reset. This product allows three reset factors to be issued using the three push switches shown in Figure 2-3.

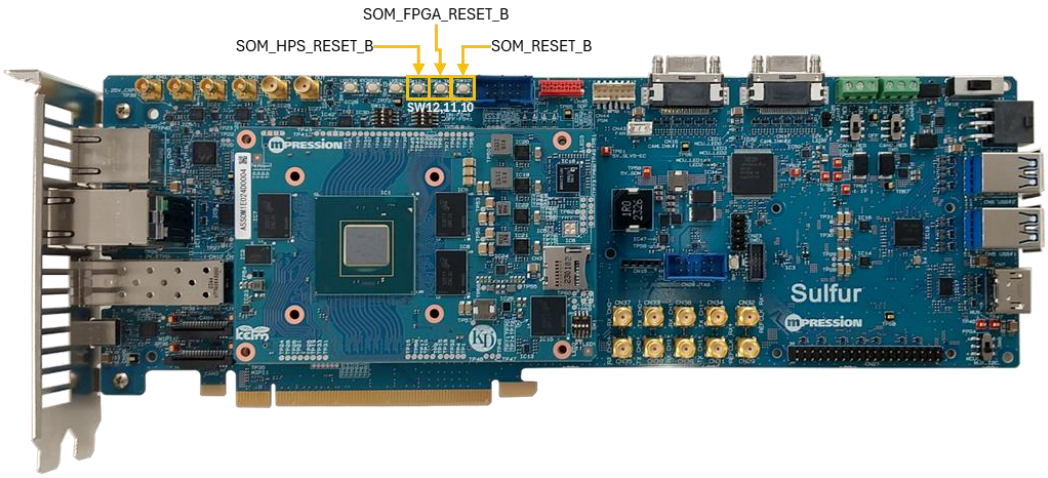


Figure 2-3 Reset Switch Board Layout

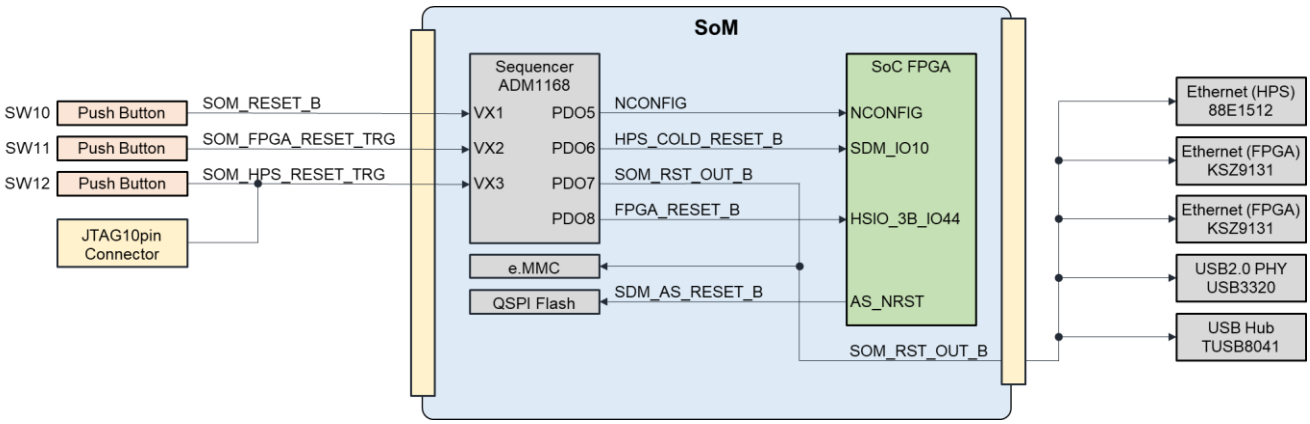


Figure 2-4 Reset Circuit

2.3.1. **Reset Timing: Re-Configuration**

Allow you to reconfiguration for this product by keeping the SOM_RESET_B signal low for 0.3ms or more. Figure 2-5 shows the timing diagram.

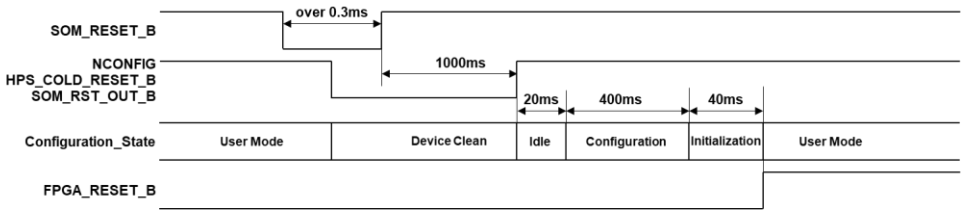


Figure 2-5 Re-Configuration Timing

2.3.2. **Reset Timing: HPS Cold Reset**

Allow you to reset for HPS on this product by keeping the SOM_HPS_RESET_TRG_B signal low for 0.3ms or more. Figure 2-6 shows the timing diagram.

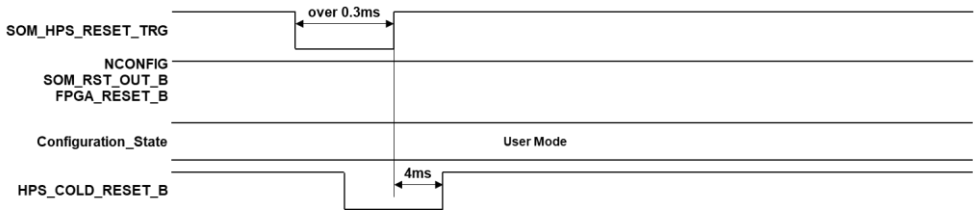


Figure 2-6 HPS Cold Reset Timing

2.3.3. **Reset Timing: FPGA Reset**

Allow you to reset for FPGA on this product by keeping the SOM_FPGA_RESET_TRG_B signal low for 0.3ms or more. Figure 2-7 shows the timing diagram.

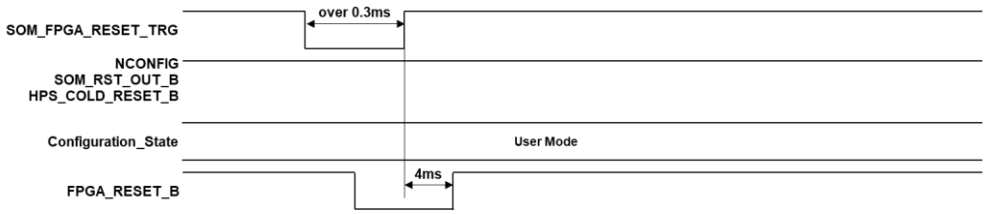


Figure 2-7 FPGA Reset Timing

2.4. **Clock Circuit**

Figure 2-8 shows the Clock Circuit of this product.

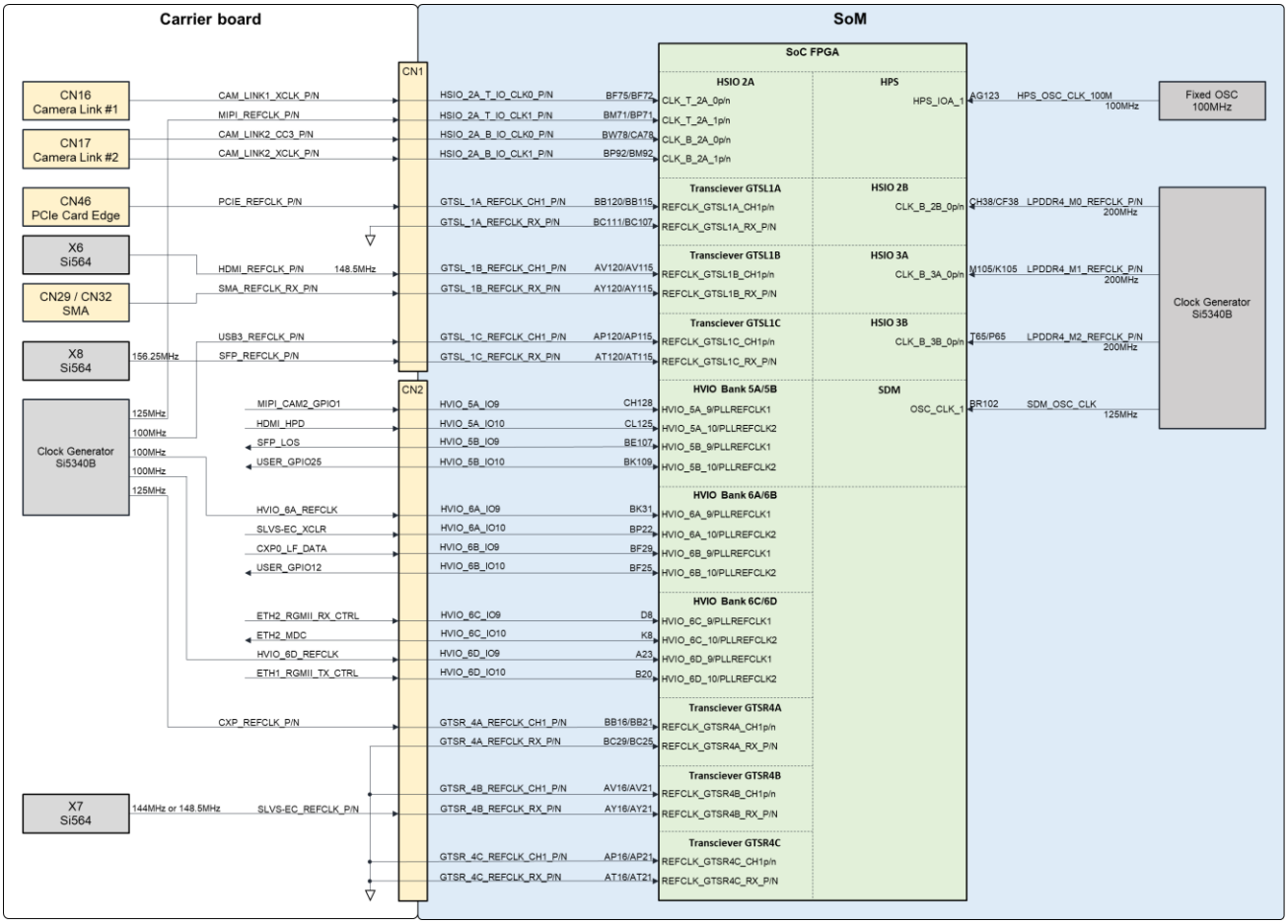


Figure 2-8 Clock Circuit

2.5. **Ethernet**

This product is equipped with 1-channel Ethernet Circuit on the HPS side and 1-channels on the FPGA side. The board layout of the Ethernet Connector is shown in Figure 2-9.

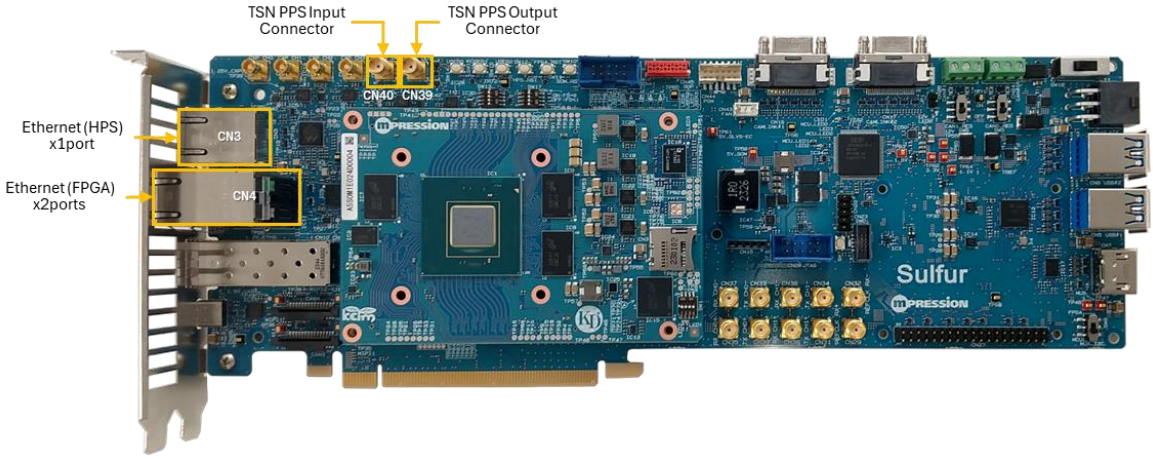


Figure 2-9 Ethernet Connector Layout

2.5.1. **Ethernet HPS (CN3)**

Figure 2-10 shows the HPS side Ethernet Circuit of this product, and Table 2-4 lists the pin assignment.

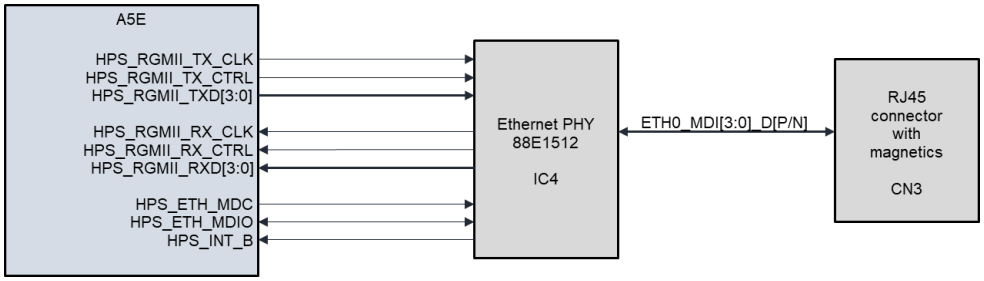


Figure 2-10 Ethernet HPS Circuit

Table 2-4 Ethernet HPS Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
HPS_RGMII_RX_CLK	CN1.C8	HPS_RGMII_RX_CLK	M124	1.8-V LVCMOS
HPS_RGMII_RX_CTRL	CN1.C9	HPS_RGMII_RX_CTRL	AB127	1.8-V LVCMOS
HPS_RGMII_RXD0	CN1.C11	HPS_RGMII_RXD0	H127	1.8-V LVCMOS
HPS_RGMII_RXD1	CN1.C12	HPS_RGMII_RXD1	AB124	1.8-V LVCMOS
HPS_RGMII_RXD2	CN1.C14	HPS_RGMII_RXD2	F124	1.8-V LVCMOS
HPS_RGMII_RXD3	CN1.C15	HPS_RGMII_RXD3	D124	1.8-V LVCMOS
HPS_RGMII_TX_CLK	CN1.D7	HPS_RGMII_TX_CLK	M127	1.8-V LVCMOS
HPS_RGMII_TX_CTRL	CN1.D8	HPS_RGMII_TX_CTRL	K127	1.8-V LVCMOS
HPS_RGMII_TXD0	CN1.D10	HPS_RGMII_TXD0	K124	1.8-V LVCMOS
HPS_RGMII_TXD1	CN1.D11	HPS_RGMII_TXD1	Y127	1.8-V LVCMOS
HPS_RGMII_TXD2	CN1.D13	HPS_RGMII_TXD2	F127	1.8-V LVCMOS
HPS_RGMII_TXD3	CN1.D14	HPS_RGMII_TXD3	Y124	1.8-V LVCMOS
HPS_ETH_MDIO	CN1.D16	HPS_ETH_MDIO	R134	1.8-V LVCMOS
HPS_ETH_MDC	CN1.D17	HPS_ETH_MDC	AG115	1.8-V LVCMOS

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
HPS_ETH_INT_B	CN1.D19	HPS_ETH_INT_B	U135	1.8-V LVCMOS

2.5.2. **Ethernet FPGA (CN4)**

Figure 2-11 shows the FPGA side Ethernet Circuit of this product, and Table 2-5 lists the pin assignment.

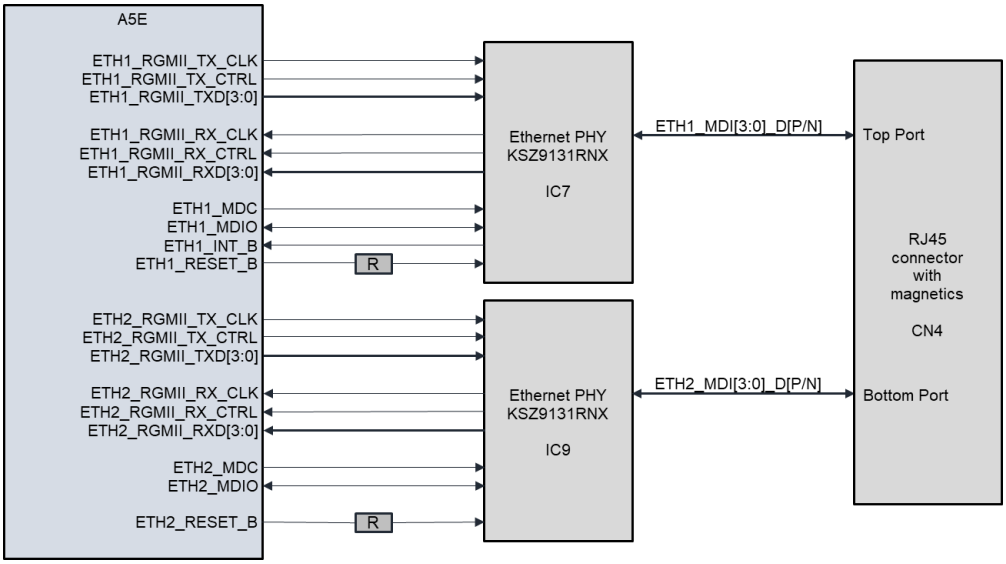


Figure 2-11 Ethernet FPGA Circuit

Note: By default, the reset terminals of the Ethernet PHY (IC7, IC9) are both connected to SOM_RST_OUT_B_1V8. It is also possible to connect to the outputs from FPGA (ETH1_RESET_B and ETH2_RESET_B) by replacing the 0-Ohm resistors.

Table 2-5 Ethernet FPGA Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
ETH1_INT_B	CN2.B13	HVIO_6D_IO17	A39	ETH1_INT_B
ETH1_MDC	CN2.B20	HVIO_6D_IO12	B26	ETH1_MDC
ETH1_MDIO	CN2.A14	HVIO_6D_IO18	B35	ETH1_MDIO
ETH1_RESET_B	CN2.B26	HVIO_6D_IO4	B11	ETH1_RESET_B
ETH1_RGMII_RX_CLK	CN2.B19	HVIO_6D_IO11	B23	ETH1_RGMII_RX_CLK
ETH1_RGMII_RX_CTRL	CN2.A21	HVIO_6D_IO10	B20	ETH1_RGMII_RX_CTRL
ETH1_RGMII_RXD0	CN2.B22	HVIO_6D_IO7	A20	ETH1_RGMII_RXD0
ETH1_RGMII_RXD1	CN2.A23	HVIO_6D_IO6	A14	ETH1_RGMII_RXD1
ETH1_RGMII_RXD2	CN2.A24	HVIO_6D_IO5	B14	ETH1_RGMII_RXD2
ETH1_RGMII_RXD3	CN2.B23	HVIO_6D_IO8	A17	ETH1_RGMII_RXD3
ETH1_RGMII_TX_CLK	CN2.A15	HVIO_6D_IO19	D34	ETH1_RGMII_TX_CLK
ETH1_RGMII_TX_CTRL	CN2.B14	HVIO_6D_IO20	B39	ETH1_RGMII_TX_CTRL
ETH1_RGMII_TXD0	CN2.B16	HVIO_6D_IO15	A35	ETH1_RGMII_TXD0
ETH1_RGMII_TXD1	CN2.A17	HVIO_6D_IO14	A30	ETH1_RGMII_TXD1
ETH1_RGMII_TXD2	CN2.A18	HVIO_6D_IO13	B30	ETH1_RGMII_TXD2
ETH1_RGMII_TXD3	CN2.B17	HVIO_6D_IO16	A33	ETH1_RGMII_TXD3
ETH2_INT_B	CN2.D23	HVIO_6C_IO17	G2	ETH2_INT_B
ETH2_MDC	CN2.C27	HVIO_6C_IO10	K8	ETH2_MDC
ETH2_MDIO	CN2.C26	HVIO_6C_IO12	H8	ETH2_MDIO

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
ETH2_RESET_B	CN2.D26	HVIO_6C_IO18	J2	ETH2_RESET_B
ETH2_RGMII_RX_CLK	CN2.D19	HVIO_6C_IO11	F8	ETH2_RGMII_RX_CLK
ETH2_RGMII_RX_CTRL	CN2.D20	HVIO_6C_IO9	D8	ETH2_RGMII_RX_CTRL
ETH2_RGMII_RXD0	CN2.C17	HVIO_6C_IO6	D15	ETH2_RGMII_RXD0
ETH2_RGMII_RXD1	CN2.C18	HVIO_6C_IO8	F15	ETH2_RGMII_RXD1
ETH2_RGMII_RXD2	CN2.D17	HVIO_6C_IO5	H18	ETH2_RGMII_RXD2
ETH2_RGMII_RXD3	CN2.C15	HVIO_6C_IO7	F18	ETH2_RGMII_RXD3
ETH2_RGMII_TX_CLK	CN2.C24	HVIO_6C_IO20	G1	ETH2_RGMII_TX_CLK
ETH2_RGMII_TX_CTRL	CN2.C23	HVIO_6C_IO19	J1	ETH2_RGMII_TX_CTRL
ETH2_RGMII_TXD0	CN2.D25	HVIO_6C_IO16	K4	ETH2_RGMII_TXD0
ETH2_RGMII_TXD1	CN2.C21	HVIO_6C_IO13	C2	ETH2_RGMII_TXD1
ETH2_RGMII_TXD2	CN2.D22	HVIO_6C_IO15	F4	ETH2_RGMII_TXD2
ETH2_RGMII_TXD3	CN2.C20	HVIO_6C_IO14	D4	ETH2_RGMII_TXD3

2.5.3. **TSN Connector (CN39, CN40)**

The TSN Connector is used for input and output of TSN Synchronization Signals. Figure 2-12 shows the TSN Circuit of this product and Table 2-6 lists the pin assignment.

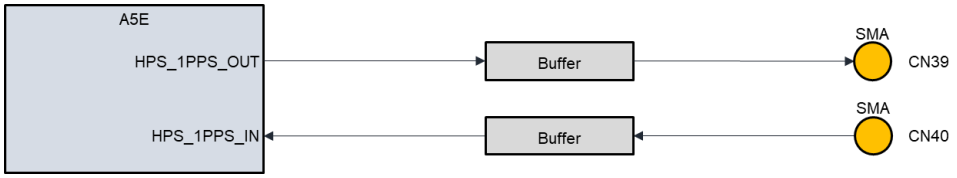


Figure 2-12 TSN Circuit

Table 2-6 TSN Synchronization Signals Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
HPS_1PPS_OUT_1V8	CN1.B19	HPS_1PPS_OUT	U134	1.8-V LVCMOS
HPS_1PPS_IN_1V8	CN1.B20	HPS_1PPS_IN	AL120	1.8-V LVCMOS

2.6. **USB 3.1 / 2.0**

Figure 2-13 shows the board layout of USB Connector on this product, Figure 2-14 shows the circuit block, and Table 2-7 lists the pin assignment.

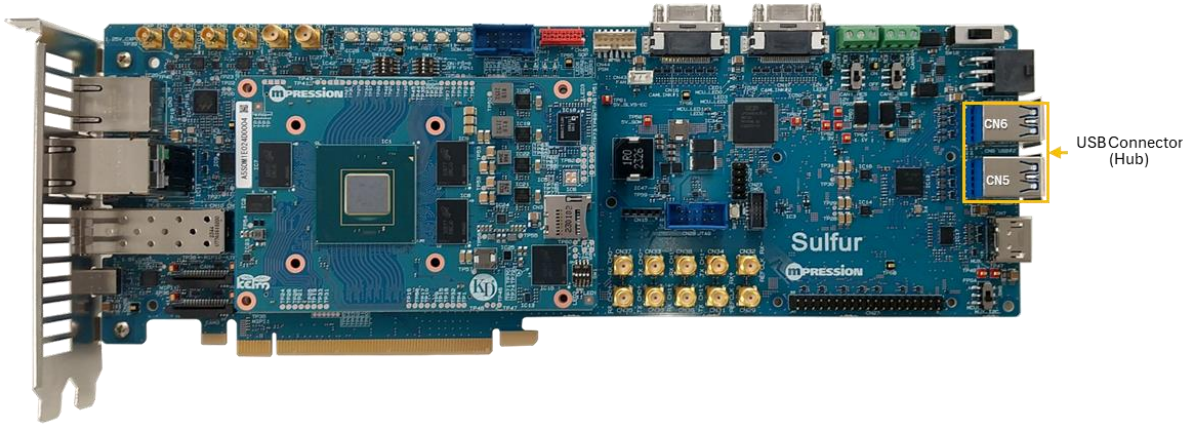


Figure 2-13 USB Connector Layout

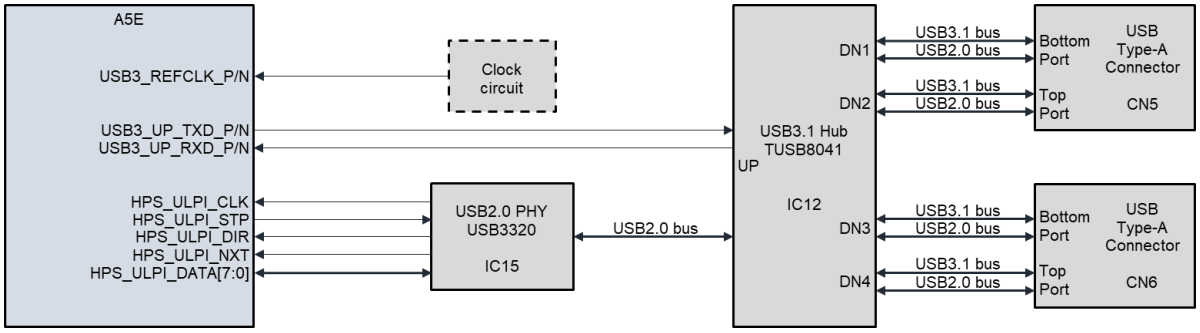


Figure 2-14 USB Circuit

Table 2-7 USB Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
HPS_ULPI_CLK	CN1.B11	HPS_ULPI_CLK	P132	1.8-V LVCMOS
HPS_ULPI_DATA0	CN1.A11	HPS_ULPI_DATA0	AD135	1.8-V LVCMOS
HPS_ULPI_DATA1	CN1.A9	HPS_ULPI_DATA1	M132	1.8-V LVCMOS
HPS_ULPI_DATA2	CN1.B7	HPS_ULPI_DATA2	K132	1.8-V LVCMOS
HPS_ULPI_DATA3	CN1.A6	HPS_ULPI_DATA3	AG129	1.8-V LVCMOS
HPS_ULPI_DATA4	CN1.B10	HPS_ULPI_DATA4	J134	1.8-V LVCMOS
HPS_ULPI_DATA5	CN1.A5	HPS_ULPI_DATA5	AG120	1.8-V LVCMOS
HPS_ULPI_DATA6	CN1.B8	HPS_ULPI_DATA6	G134	1.8-V LVCMOS
HPS_ULPI_DATA7	CN1.A8	HPS_ULPI_DATA7	G135	1.8-V LVCMOS
HPS_ULPI_DIR	CN1.B14	HPS_ULPI_DIR	J135	1.8-V LVCMOS
HPS_ULPI_NXT	CN1.A12	HPS_ULPI_NXT	AD134	1.8-V LVCMOS
HPS_ULPI_STP	CN1.B13	HPS_ULPI_STP	L135	1.8-V LVCMOS
USB_ID_3V3	CN2.B87	HVIO_5A_IO1	CD134	3.3-V LVCMOS
USB_VBUS_DET_3V3	CN2.A92	HVIO_5A_IO4	CG135	3.3-V LVCMOS
USB3_REFCLK_N	CN1.A41	GTSL_1C_REFCLK_CH1_N	AP115	Current Mode Logic (CML)
USB3_REFCLK_P	CN1.A42	GTSL_1C_REFCLK_CH1_P	AP120	Current Mode Logic (CML)
USB3_UP_RXD_N	CN1.D35	GTSL_1C_RX_CH2_N	AM133	High Speed Differential I/O

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
USB3_UP_RXD_P	CN1.D36	GTSL_1C_RX_CH2_P	AM135	High Speed Differential I/O
USB3_UP_TXD_N	CN1.C33	GTSL_1C_TX_CH2_N	AN126	High Speed Differential I/O
USB3_UP_TXD_P	CN1.C34	GTSL_1C_TX_CH2_P	AN129	High Speed Differential I/O

2.7. **10GbE**

Figure 2-15 shows the board layout of 10GbE Connector on this product, Figure 2-16 shows the circuit block, Table 2-8 lists the pin assignment.

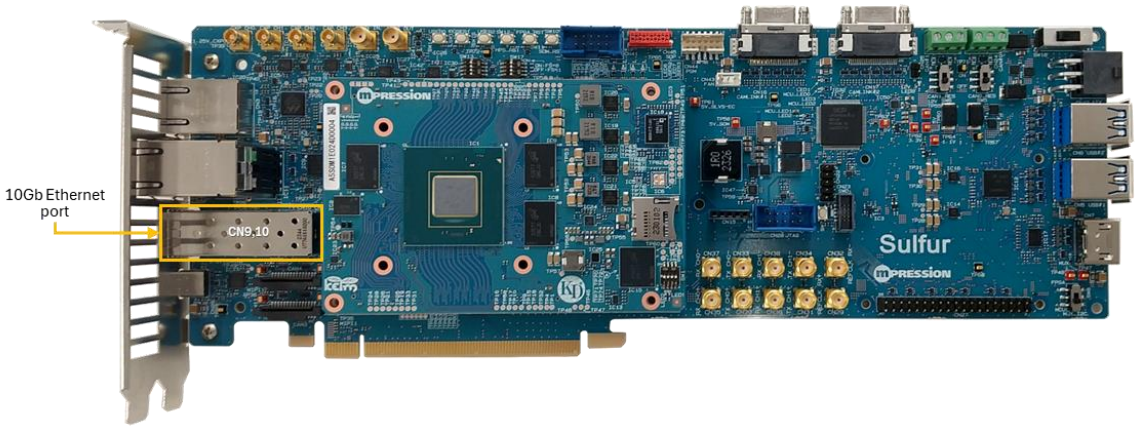


Figure 2-15 10GbE Connector Layout

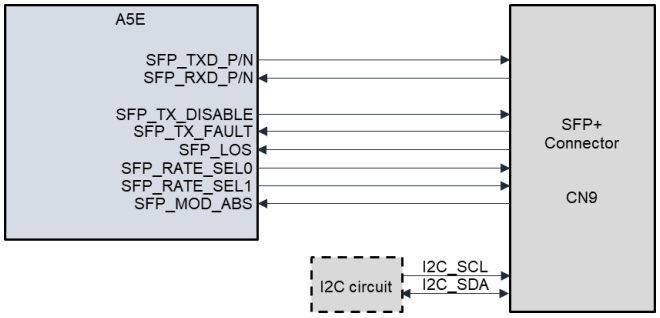


Figure 2-16 10GbE Circuit

Table 2-8 10GbE Circuit Pin Assignments

Signal Name	BtoB pin	SoM Pin Name	A5E Pin	I/O Standard
SFP_TXD_N	CN1.A33	GTSL_1C_TX_CH3_N	AL126	High Speed Differential I/O
SFP_TXD_P	CN1.A34	GTSL_1C_TX_CH3_P	AL129	High Speed Differential I/O
SFP_RXD_N	CN1.B35	GTSL_1C_RX_CH3_N	AK133	High Speed Differential I/O
SFP_RXD_P	CN1.B36	GTSL_1C_RX_CH3_P	AK135	High Speed Differential I/O
SFP_REFCLK_N	CN1.C41	GTSL_1C_REFCLK_RX_N	AT115	Current Mode Logic (CML)
SFP_REFCLK_P	CN1.C42	GTSL_1C_REFCLK_RX_P	AT120	Current Mode Logic (CML)
SFP_TX_FAULT	CN2.D96	HVIO_5B_IO1	BF111	3.3-V LVCMOS
SFP_MOD_ABS	CN2.C98	HVIO_5B_IO11	BE111	3.3-V LVCMOS
SFP_TX_DISABLE	CN2.C96	HVIO_5B_IO20	BF120	3.3-V LVCMOS
SFP_RATE_SEL0	CN2.D97	HVIO_5B_IO3	BE115	3.3-V LVCMOS
SFP_RATE_SEL1	CN2.C95	HVIO_5B_IO4	BF115	3.3-V LVCMOS
SFP_LOS	CN2.C99	HVIO_5B_IO9	BE107	3.3-V LVCMOS

2.8. **HDMI**

Figure 2-17 shows the board layout of HDMI Connector on this product, Figure 2-18 shows the circuit block, Table 2-9 lists the pin assignment.

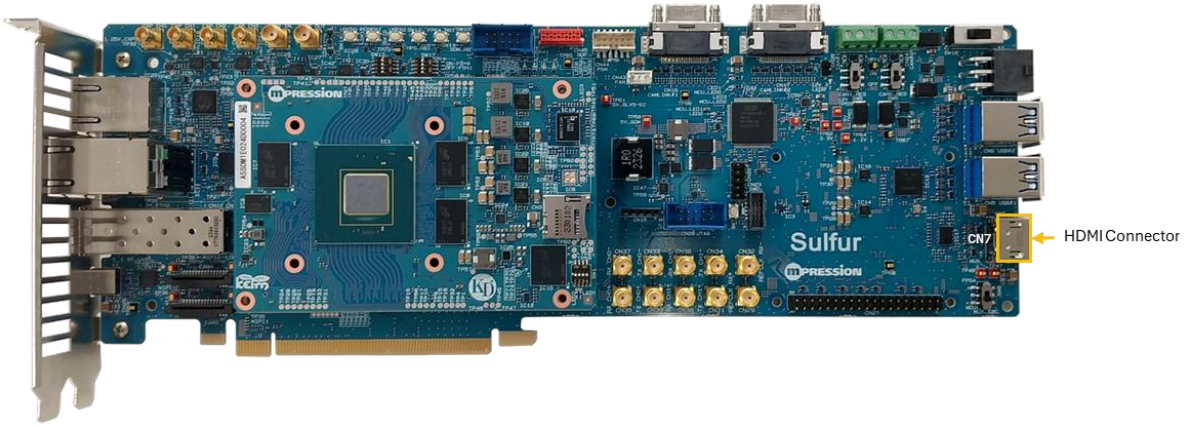


Figure 2-17 HDMI Connector Layout

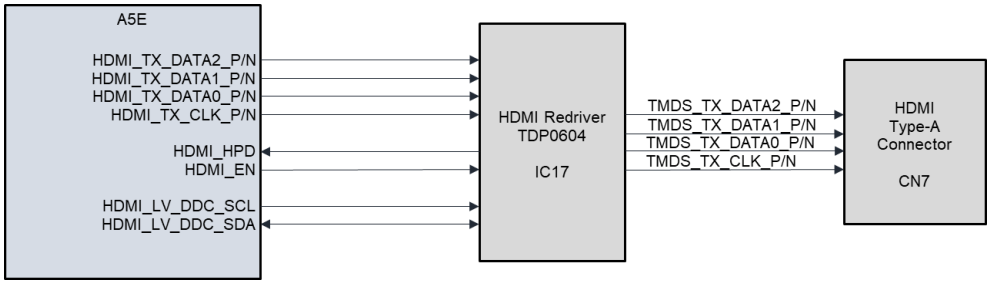


Figure 2-18 HDMI Circuit

Table 2-9 HDMI Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
HDMI_TX_DATA2_P	CN1.D44	GTSL_1B_TX_CH2_P	BA129	High Speed Differential I/O
HDMI_TX_DATA2_N	CN1.D43	GTSL_1B_TX_CH2_N	BA126	High Speed Differential I/O
HDMI_TX_DATA1_P	CN1.B48	GTSL_1B_TX_CH1_P	BC129	High Speed Differential I/O
HDMI_TX_DATA1_N	CN1.B47	GTSL_1B_TX_CH1_N	BC126	High Speed Differential I/O
HDMI_TX_DATA0_P	CN1.D48	GTSL_1B_TX_CH0_P	BE129	High Speed Differential I/O
HDMI_TX_DATA0_N	CN1.D47	GTSL_1B_TX_CH0_N	BE126	High Speed Differential I/O
HDMI_TX_CLK_P	CN1.B44	GTSL_1B_TX_CH3_P	AW129	High Speed Differential I/O
HDMI_TX_CLK_N	CN1.B43	GTSL_1B_TX_CH3_N	AW126	High Speed Differential I/O
HDMI_REFCLK_P	CN1.B52	GTSL_1B_REFCLK_CH1_P	AV120	Current Mode Logic (CML)
HDMI_REFCLK_N	CN1.B51	GTSL_1B_REFCLK_CH1_N	AV115	Current Mode Logic (CML)
HDMI_LV_DDC_SDA_3V3	CN2.A96	HVIO_5A_IO17	CL128	3.3-V LVCMOS
HDMI_LV_DDC_SCL_3V3	CN2.B97	HVIO_5A_IO20	CK128	3.3-V LVCMOS
HDMI_HPD_3V3	CN2.B100	HVIO_5A_IO10	CL125	3.3-V LVCMOS
HDMI_EN_3V3	CN2.B99	HVIO_5A_IO19	CK125	3.3-V LVCMOS

2.9. **MIPI**

Figure 2-19 shows the board layout of MIPI on this product, Figure 2-20 shows the circuit block, Table 2-10 lists the pin assignment. When using MIPI, set HSIO_2A to 1.2V bank voltage using SW19.

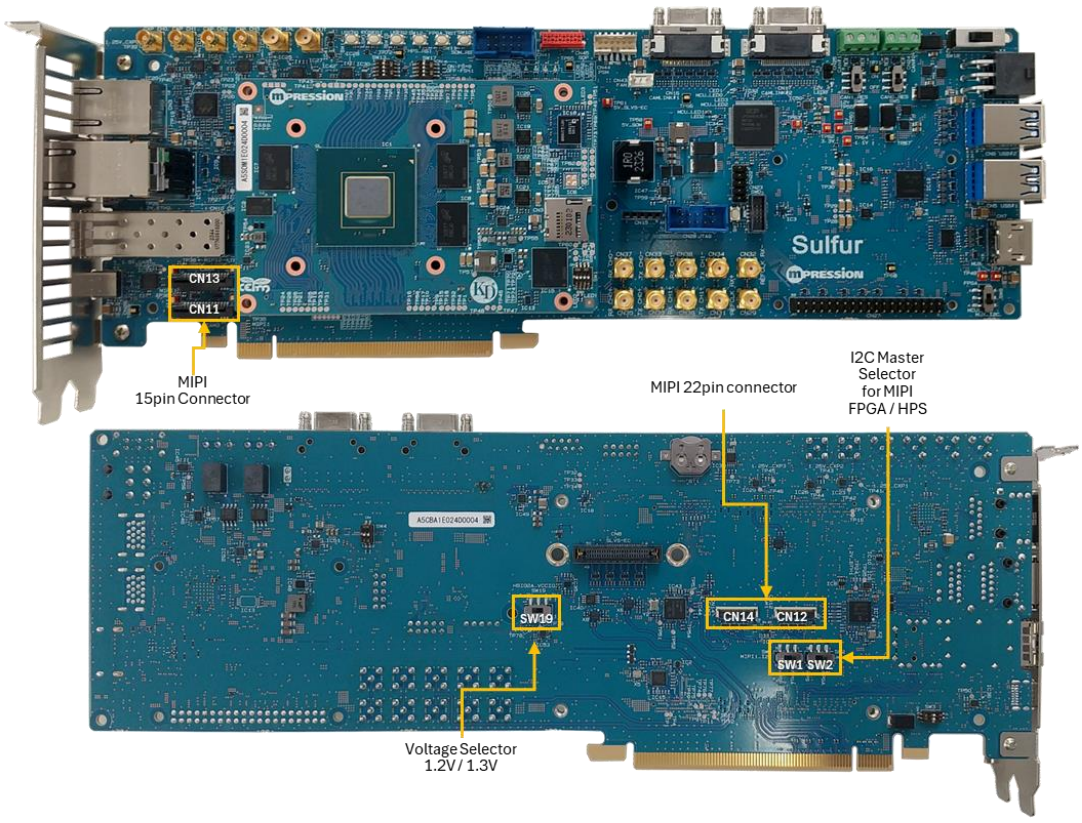


Figure 2-19 MIPI Layout

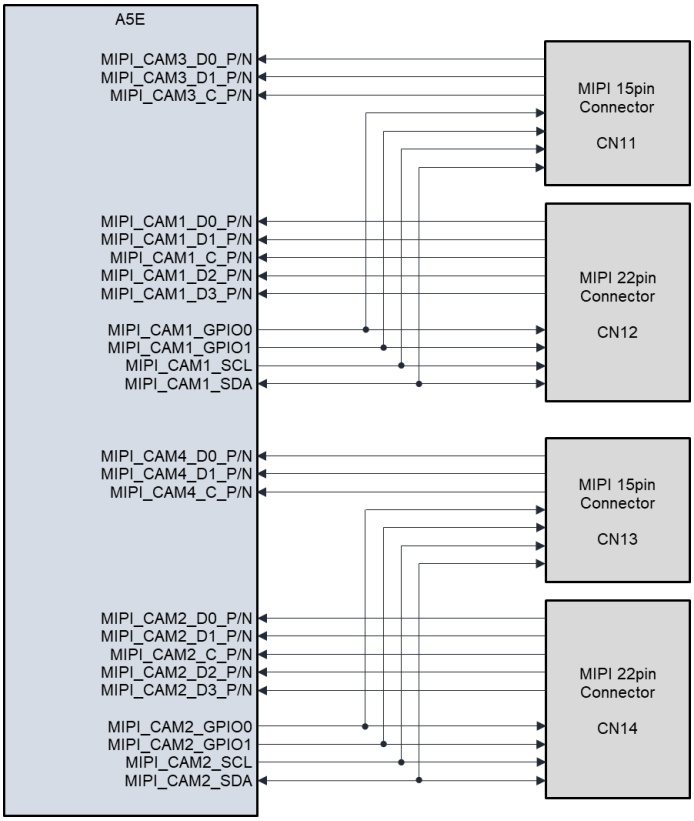


Figure 2-20 MIPI Circuit

Table 2-10 MIPI Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
MIPI_CAM1_C_N	CN1.C89	HSIO_2A_T_IO_N4	CF69	DPHY
MIPI_CAM1_C_P	CN1.C90	HSIO_2A_T_IO_P4	CH69	DPHY
MIPI_CAM1_D0_N	CN1.C83	HSIO_2A_T_IO_N6	CH71	DPHY
MIPI_CAM1_D0_P	CN1.C84	HSIO_2A_T_IO_P6	CF71	DPHY
MIPI_CAM1_D1_N	CN1.C86	HSIO_2A_T_IO_N5	CA71	DPHY
MIPI_CAM1_D1_P	CN1.C87	HSIO_2A_T_IO_P5	CC71	DPHY
MIPI_CAM1_D2_N	CN1.C95	HSIO_2A_T_IO_N3	CC62	DPHY
MIPI_CAM1_D2_P	CN1.C96	HSIO_2A_T_IO_P3	CA62	DPHY
MIPI_CAM1_D3_N	CN1.C92	HSIO_2A_T_IO_N2	CH62	DPHY
MIPI_CAM1_D3_P	CN1.C93	HSIO_2A_T_IO_P2	CF62	DPHY
MIPI_CAM1_GPIO0_3V3	CN2.B88	HVIO_5A_IO15	CA118	3.3-V LVCMOS
MIPI_CAM1_GPIO1_3V3	CN2.A86	HVIO_5A_IO12	CF118	3.3-V LVCMOS
MIPI_CAM1_SCL_3V3	CN2.B84	HVIO_5A_IO11	CF121	3.3-V LVCMOS
MIPI_CAM1_SDA_3V3	CN2.A83	HVIO_5A_IO7	CF128	3.3-V LVCMOS
MIPI_CAM2_C_N	CN1.D90	HSIO_2A_T_IO_N10	CA69	DPHY
MIPI_CAM2_C_P	CN1.D91	HSIO_2A_T_IO_P10	BW69	DPHY
MIPI_CAM2_D0_N	CN1.D87	HSIO_2A_T_IO_N12	BU69	DPHY
MIPI_CAM2_D0_P	CN1.D88	HSIO_2A_T_IO_P12	BR69	DPHY
MIPI_CAM2_D1_N	CN1.D84	HSIO_2A_T_IO_N11	BU71	DPHY
MIPI_CAM2_D1_P	CN1.D85	HSIO_2A_T_IO_P11	BR71	DPHY
MIPI_CAM2_D2_N	CN1.D93	HSIO_2A_T_IO_N9	BR62	DPHY
MIPI_CAM2_D2_P	CN1.D94	HSIO_2A_T_IO_P9	BU62	DPHY
MIPI_CAM2_D3_N	CN1.D96	HSIO_2A_T_IO_N8	BR59	DPHY
MIPI_CAM2_D3_P	CN1.D97	HSIO_2A_T_IO_P8	BU59	DPHY

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
MIPI_CAM2_GPIO0_3V3	CN2.B85	HVIO_5A_IO16	BW118	3.3-V LVCMOS
MIPI_CAM2_GPIO1_3V3	CN2.A84	HVIO_5A_IO9	CH128	3.3-V LVCMOS
MIPI_CAM2_SCL_3V3	CN2.B82	HVIO_5A_IO14	BR118	3.3-V LVCMOS
MIPI_CAM2_SDA_3V3	CN2.B81	HVIO_5A_IO13	BU118	3.3-V LVCMOS
MIPI_CAM3_C_N	CN1.D69	HSIO_2A_B_IO_N16	CF89	DPHY
MIPI_CAM3_C_P	CN1.D70	HSIO_2A_B_IO_P16	CH89	DPHY
MIPI_CAM3_D0_N	CN1.D66	HSIO_2A_B_IO_N18	CA92	DPHY
MIPI_CAM3_D0_P	CN1.D67	HSIO_2A_B_IO_P18	CC92	DPHY
MIPI_CAM3_D1_N	CN1.D63	HSIO_2A_B_IO_N17	CH92	DPHY
MIPI_CAM3_D1_P	CN1.D64	HSIO_2A_B_IO_P17	CF92	DPHY
MIPI_CAM4_C_N	CN1.A77	HSIO_2A_B_IO_N22	CK88	DPHY
MIPI_CAM4_C_P	CN1.A78	HSIO_2A_B_IO_P22	CL88	DPHY
MIPI_CAM4_D0_N	CN1.B75	HSIO_2A_B_IO_N24	CK94	DPHY
MIPI_CAM4_D0_P	CN1.B76	HSIO_2A_B_IO_P24	CL91	DPHY
MIPI_CAM4_D1_N	CN1.A74	HSIO_2A_B_IO_N23	CL97	DPHY
MIPI_CAM4_D1_P	CN1.A75	HSIO_2A_B_IO_P23	CK97	DPHY
MIPI_REFCLK_N	CN1.A83	HSIO_2A_T_IO_CLK1_N	BP71	1.2V True Differential Signaling
MIPI_REFCLK_P	CN1.A84	HSIO_2A_T_IO_CLK1_P	BM71	1.2V True Differential Signaling

Table 2-11 1.2V Setting of HSIO_2A Voltage Selection (SW19)

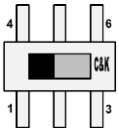
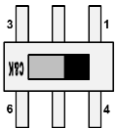
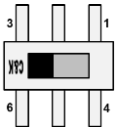
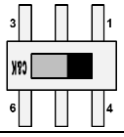
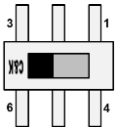
Reference	Name	Description	Drawing
SW19	HSIO_2A_VCCIO	1, 4 Side: Set Bank Voltage of HSIO_2A to 1.2V (Default)	

表 2-1 MIPI I2C Master Selection (SW1, SW2)

Reference	Name	Description	Drawing
SW1	MIPI_CAM1, CAM3 I2C Master Select	1, 4 Side: Set I2C Master to FPGA side (Default)	
		3, 6 Side: Set I2C Master to HPS side	
SW2	MIPI_CAM2, CAM4 I2C Master Select	1, 4 Side: Set I2C Master to FPGA side (Default)	
		3, 6 Side: Set I2C Master to HPS side	

2.10. **Camera Link**

Figure 2-21 shows the board layout of Camera Link on this product, Figure 2-22 shows the circuit block, Table 2-12 lists the pin assignment. When using Camera Link, set HSIO_2A to 1.3V bank voltage using SW19.

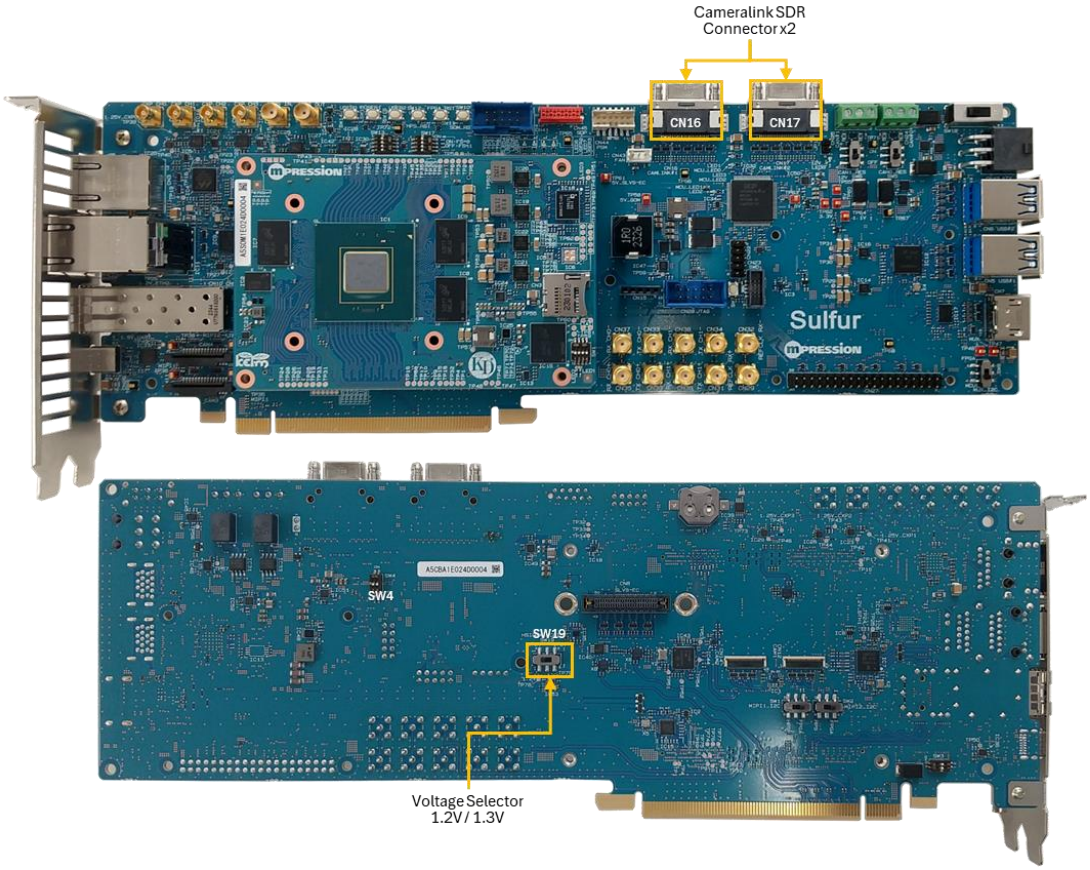


Figure 2-21 Camera Link Layout

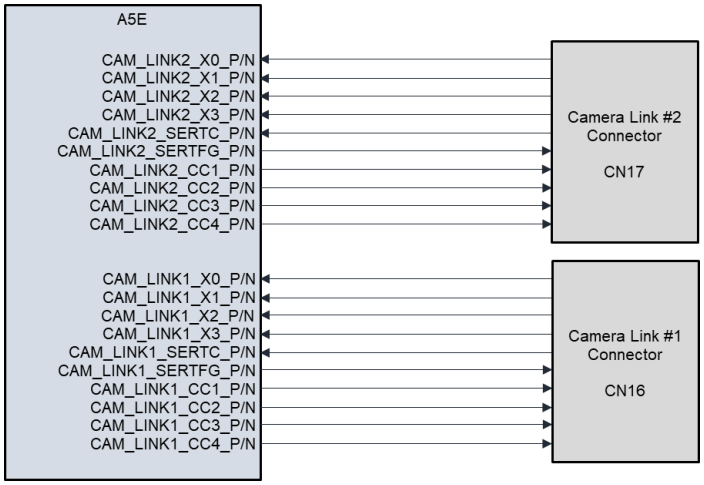
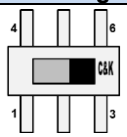


Figure 2-22 Camera Link Circuit

Table 2-12 Camera Link Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
CAM_LINK2_XCLK_P	CN1.A66	HSIO_2A_B_IO_CLK1_P	BP92	1.3V True Differential Signaling
CAM_LINK2_XCLK_N	CN1.A65	HSIO_2A_B_IO_CLK1_N	BM92	1.3V True Differential Signaling
CAM_LINK2_X3_P	CN1.B70	HSIO_2A_B_IO_P3	BM81	1.3V True Differential Signaling
CAM_LINK2_X3_N	CN1.B69	HSIO_2A_B_IO_N3	BP81	1.3V True Differential Signaling
CAM_LINK2_X2_P	CN1.B73	HSIO_2A_B_IO_P2	BH81	1.3V True Differential Signaling
CAM_LINK2_X2_N	CN1.B72	HSIO_2A_B_IO_N2	BH78	1.3V True Differential Signaling
CAM_LINK2_X1_P	CN1.A69	HSIO_2A_B_IO_P1	BM78	1.3V True Differential Signaling
CAM_LINK2_X1_N	CN1.A68	HSIO_2A_B_IO_N1	BK78	1.3V True Differential Signaling
CAM_LINK2_X0_P	CN1.B67	HSIO_2A_B_IO_P4	BK89	1.3V True Differential Signaling
CAM_LINK2_X0_N	CN1.B66	HSIO_2A_B_IO_N4	BM89	1.3V True Differential Signaling
CAM_LINK2_SERTFG_P	CN1.C69	HSIO_2A_B_IO_P12	BR89	1.3V True Differential Signaling
CAM_LINK2_SERTFG_N	CN1.C68	HSIO_2A_B_IO_N12	BU89	1.3V True Differential Signaling
CAM_LINK2_SERTC_P	CN1.C66	HSIO_2A_B_IO_P11	BR92	1.3V True Differential Signaling
CAM_LINK2_SERTC_N	CN1.C65	HSIO_2A_B_IO_N11	BU92	1.3V True Differential Signaling
CAM_LINK2_CC4_P	CN1.C75	HSIO_2A_B_IO_P9	BR81	1.3V True Differential Signaling
CAM_LINK2_CC4_N	CN1.C74	HSIO_2A_B_IO_N9	BU81	1.3V True Differential Signaling
CAM_LINK2_CC3_P	CN1.A72	HSIO_2A_B_IO_CLK0_P	BW78	1.3V True Differential Signaling
CAM_LINK2_CC3_N	CN1.A71	HSIO_2A_B_IO_CLK0_N	CA78	1.3V True Differential Signaling
CAM_LINK2_CC2_P	CN1.C78	HSIO_2A_B_IO_P8	BR78	1.3V True Differential Signaling
CAM_LINK2_CC2_N	CN1.C77	HSIO_2A_B_IO_N8	BU78	1.3V True Differential Signaling
CAM_LINK2_CC1_P	CN1.C72	HSIO_2A_B_IO_P10	BW89	1.3V True Differential Signaling
CAM_LINK2_CC1_N	CN1.C71	HSIO_2A_B_IO_N10	CA89	1.3V True Differential Signaling
CAM_LINK1_XCLK_P	CN1.A87	HSIO_2A_T_IO_CLK0_P	BF75	1.3V True Differential Signaling
CAM_LINK1_XCLK_N	CN1.A86	HSIO_2A_T_IO_CLK0_N	BF72	1.3V True Differential Signaling
CAM_LINK1_X3_P	CN1.B91	HSIO_2A_T_IO_P14	BH62	1.3V True Differential Signaling
CAM_LINK1_X3_N	CN1.B90	HSIO_2A_T_IO_N14	BH59	1.3V True Differential Signaling
CAM_LINK1_X2_P	CN1.B88	HSIO_2A_T_IO_P15	BM62	1.3V True Differential Signaling
CAM_LINK1_X2_N	CN1.B87	HSIO_2A_T_IO_N15	BP62	1.3V True Differential Signaling
CAM_LINK1_X1_P	CN1.B85	HSIO_2A_T_IO_P16	BM69	1.3V True Differential Signaling
CAM_LINK1_X1_N	CN1.B84	HSIO_2A_T_IO_N16	BK69	1.3V True Differential Signaling
CAM_LINK1_X0_P	CN1.B82	HSIO_2A_T_IO_P17	BH69	1.3V True Differential Signaling
CAM_LINK1_X0_N	CN1.B81	HSIO_2A_T_IO_N17	BH71	1.3V True Differential Signaling
CAM_LINK1_SERTFG_P	CN1.A96	HSIO_2A_T_IO_P24	BE96	1.3V True Differential Signaling
CAM_LINK1_SERTFG_N	CN1.A95	HSIO_2A_T_IO_N24	BE93	1.3V True Differential Signaling
CAM_LINK1_SERTC_P	CN1.B94	HSIO_2A_T_IO_P13	BM59	1.3V True Differential Signaling
CAM_LINK1_SERTC_N	CN1.B93	HSIO_2A_T_IO_N13	BK59	1.3V True Differential Signaling
CAM_LINK1_CC4_P	CN1.A93	HSIO_2A_T_IO_P20	BE79	1.3V True Differential Signaling
CAM_LINK1_CC4_N	CN1.A92	HSIO_2A_T_IO_N20	BE75	1.3V True Differential Signaling
CAM_LINK1_CC3_P	CN1.A90	HSIO_2A_T_IO_P21	BE83	1.3V True Differential Signaling
CAM_LINK1_CC3_N	CN1.A89	HSIO_2A_T_IO_N21	BF83	1.3V True Differential Signaling
CAM_LINK1_CC2_P	CN1.B100	HSIO_2A_T_IO_P22	BF86	1.3V True Differential Signaling
CAM_LINK1_CC2_N	CN1.B99	HSIO_2A_T_IO_N22	BE86	1.3V True Differential Signaling
CAM_LINK1_CC1_P	CN1.A99	HSIO_2A_T_IO_P23	BF93	1.3V True Differential Signaling
CAM_LINK1_CC1_N	CN1.A98	HSIO_2A_T_IO_N23	BF90	1.3V True Differential Signaling

Table 2-13 1.3V Setting of HSIO_2A Voltage Selection (SW19)

Reference	Name	Description	Drawing
SW19	HSIO_2A_VCCIO	3, 6 side: Set Bank Voltage of HSIO_2A to 1.3V (Default)	

2.11. **SLVS-EC**

Figure 2-23 shows the board layout of SLVS-EC on this product, Figure 2-24 shows the circuit block, Table 2-14 lists the pin assignment.

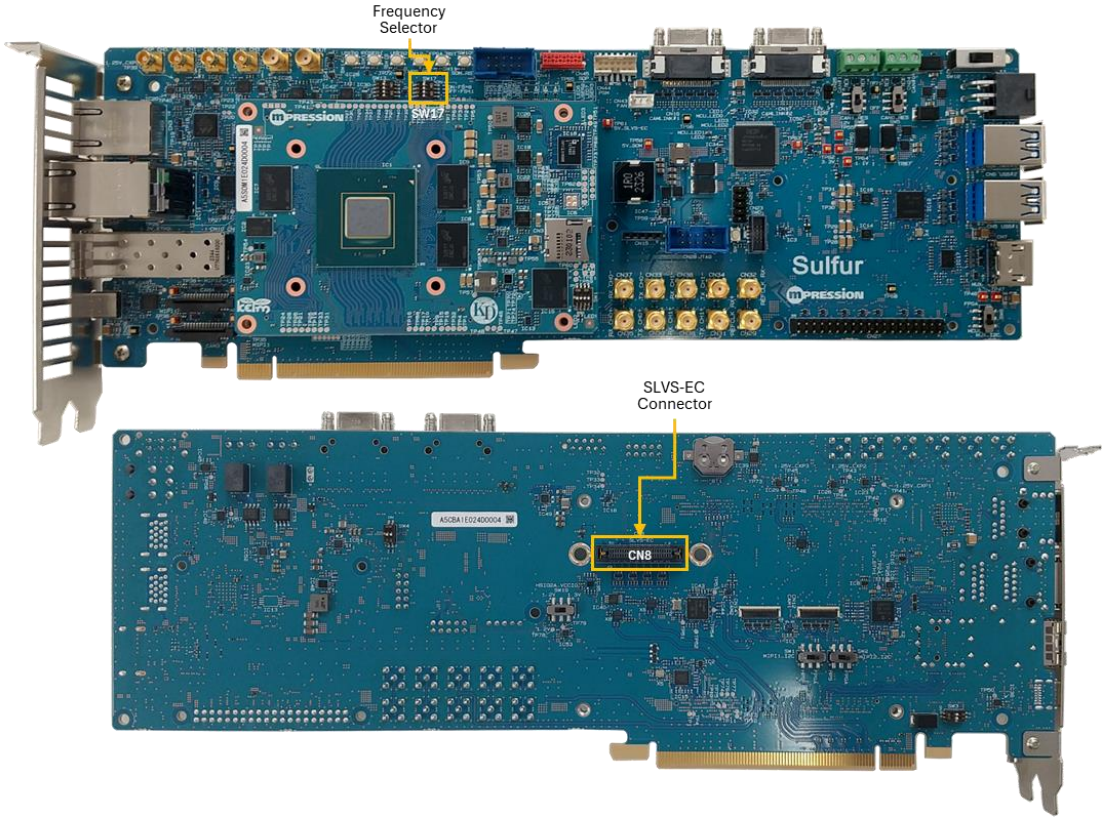


Figure 2-23 SLVS-EC Layout

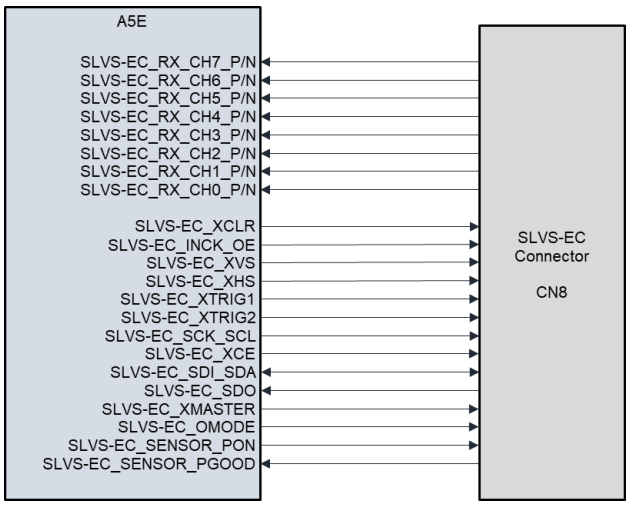


Figure 2-24 SLVS-EC Circuit

Table 2-14 SLVS-EC Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
SLVS-EC_XVS_1V8	CN2.B66	HVIO_6A_IO17	BM22	1.8-V LVCMOS
SLVS-EC_XTRIG2_1V8	CN2.A65	HVIO_6A_IO19	BK19	1.8-V LVCMOS
SLVS-EC_XTRIG1_1V8	CN2.A66	HVIO_6A_IO15	BW19	1.8-V LVCMOS
SLVS-EC_XMASTER_1V8	CN2.B67	HVIO_6A_IO18	CF12	1.8-V LVCMOS
SLVS-EC_XHS_1V8	CN2.A68	HVIO_6A_IO13	CH12	1.8-V LVCMOS
SLVS-EC_XCLR_1V8	CN2.B70	HVIO_6A_IO10	BP22	1.8-V LVCMOS
SLVS-EC_XCE_1V8	CN2.B69	HVIO_6A_IO20	CF9	1.8-V LVCMOS
SLVS-EC_SENSOR_PON_1V8	CN2.A72	HVIO_6A_IO7	BW28	1.8-V LVCMOS
SLVS-EC_SENSOR_PGOOD_1V8	CN2.B73	HVIO_6A_IO3	BR28	1.8-V LVCMOS
SLVS-EC_SDO_1V8	CN2.A69	HVIO_6A_IO12	BR22	1.8-V LVCMOS
SLVS-EC_SDI_SDA_1V8	CN2.B72	HVIO_6A_IO14	BU22	1.8-V LVCMOS
SLVS-EC_SCK_SCL_1V8	CN2.A71	HVIO_6A_IO1	BU28	1.8-V LVCMOS
SLVS-EC_RX_CH7_P	CN2.C34	GTSR_4C_RX_CH3_P	AM1	High Speed Differential I/O
SLVS-EC_RX_CH7_N	CN2.C33	GTSR_4C_RX_CH3_N	AM3	High Speed Differential I/O
SLVS-EC_RX_CH6_P	CN2.A34	GTSR_4C_RX_CH2_P	AP1	High Speed Differential I/O
SLVS-EC_RX_CH6_N	CN2.A33	GTSR_4C_RX_CH2_N	AP3	High Speed Differential I/O
SLVS-EC_RX_CH5_P	CN2.C38	GTSR_4C_RX_CH1_P	AT1	High Speed Differential I/O
SLVS-EC_RX_CH5_N	CN2.C37	GTSR_4C_RX_CH1_N	AT3	High Speed Differential I/O
SLVS-EC_RX_CH4_P	CN2.A38	GTSR_4C_RX_CH0_P	AV1	High Speed Differential I/O
SLVS-EC_RX_CH4_N	CN2.A37	GTSR_4C_RX_CH0_N	AV3	High Speed Differential I/O
SLVS-EC_RX_CH3_P	CN2.D44	GTSR_4B_RX_CH3_P	AY1	High Speed Differential I/O
SLVS-EC_RX_CH3_N	CN2.D43	GTSR_4B_RX_CH3_N	AY3	High Speed Differential I/O
SLVS-EC_RX_CH2_P	CN2.B44	GTSR_4B_RX_CH2_P	BB1	High Speed Differential I/O
SLVS-EC_RX_CH2_N	CN2.B43	GTSR_4B_RX_CH2_N	BB3	High Speed Differential I/O
SLVS-EC_RX_CH1_P	CN2.D48	GTSR_4B_RX_CH1_P	BD1	High Speed Differential I/O
SLVS-EC_RX_CH1_N	CN2.D47	GTSR_4B_RX_CH1_N	BD3	High Speed Differential I/O
SLVS-EC_RX_CH0_P	CN2.B48	GTSR_4B_RX_CH0_P	BF1	High Speed Differential I/O
SLVS-EC_RX_CH0_N	CN2.B47	GTSR_4B_RX_CH0_N	BF3	High Speed Differential I/O
SLVS-EC_REFCLK_P	CN2.B52	GTSR_4B_REFCLK_RX_P	AY16	Current Mode Logic (CML)
SLVS-EC_REFCLK_N	CN2.B51	GTSR_4B_REFCLK_RX_N	AY21	Current Mode Logic (CML)
SLVS-EC_OMODE_1V8	CN2.A74	HVIO_6A_IO6	BM28	1.8-V LVCMOS
SLVS-EC_INCK_OE_1V8	CN2.B76	HVIO_6A_IO11	BK28	1.8-V LVCMOS

2.11.1. **Clock Frequency Selection Switch (SW17)**

The SLVS-EC reference clock allows you to change the frequency with SW17. Table 2-15 shows the settings of the Clock Frequency Selector Switch.

Table 2-15 Clock Frequency Selector Switch

Reference	Name	Setting	Drawing
SW17	X7 FS	OFF: 148.5MHz (Default)	
		ON: 144MHz	

Note: The other bits of SW17 are for future expansion. These bits are unconnected in this product.

2.11.2. **SLVS-EC Connector (CN8)**

Connector Part Number: ERM8-025-05.0-L-DV-L-K-TR (Samtec)

Table 2-16 SLVS-EC Connector Pin Assignments

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	-
3	SLVS-EC_RX_CH0_P	4	-
5	SLVS-EC_RX_CH0_N	6	SLVS-EC_XCLR_1V8
7	GND	8	SLVS-EC_INCK_OE_1V8
9	SLVS-EC_RX_CH1_P	10	SLVS-EC_XVS_1V8
11	SLVS-EC_RX_CH1_N	12	SLVS-EC_XHS_1V8
13	GND	14	SLVS-EC_XTRIG1_1V8
15	SLVS-EC_RX_CH2_P	16	SLVS-EC_XTRIG2_1V8
17	SLVS-EC_RX_CH2_N	18	SLVS-EC_SCK_SCL_1V8
19	GND	20	SLVS-EC_XCE_1V8
21	SLVS-EC_RX_CH3_P	22	SLVS-EC_SDI_SDA_1V8
23	SLVS-EC_RX_CH3_N	24	SLVS-EC_SDO_1V8
25	GND	26	SLVS-EC_XMASTER_1V8
27	SLVS-EC_RX_CH4_P	28	pull-down
29	SLVS-EC_RX_CH4_N	30	pull-down
31	GND	32	pull-down
33	SLVS-EC_RX_CH5_P	34	SLVS-EC_OMODE_1V8
35	SLVS-EC_RX_CH5_N	36	-
37	GND	38	-
39	SLVS-EC_RX_CH6_P	40	-
41	SLVS-EC_RX_CH6_N	42	SLVS-EC_SENSOR_PON_5V0
43	GND	44	SLVS-EC_SENSOR_PGOOD_1V8
45	SLVS-EC_RX_CH7_P	46	5V_SLVS-EC
47	SLVS-EC_RX_CH7_N	48	5V_SLVS-EC
49	GND	50	5V_SLVS-EC

2.12. **CoaXPress**

Figure 2-25 shows the board layout of CoaXPress on this product, Figure 2-26 shows the circuit block, Table 2-17 lists the pin assignment.

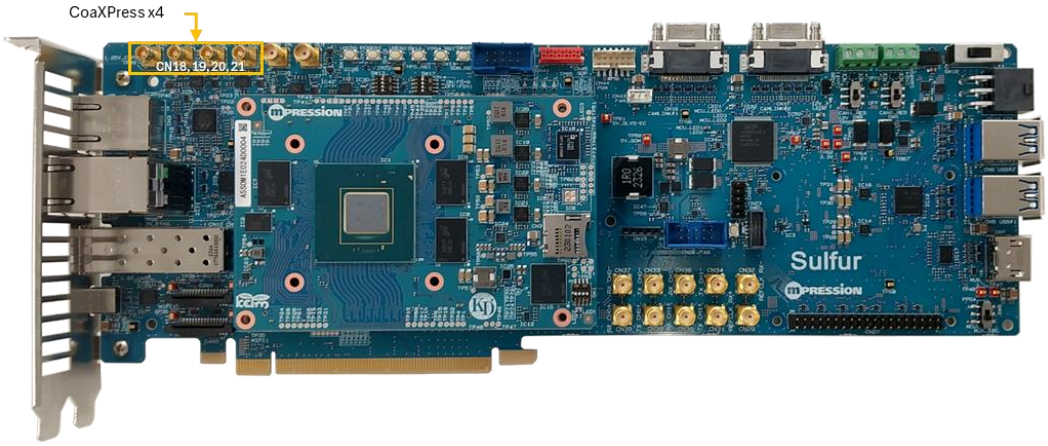


Figure 2-25 CoaXPress Connector Layout

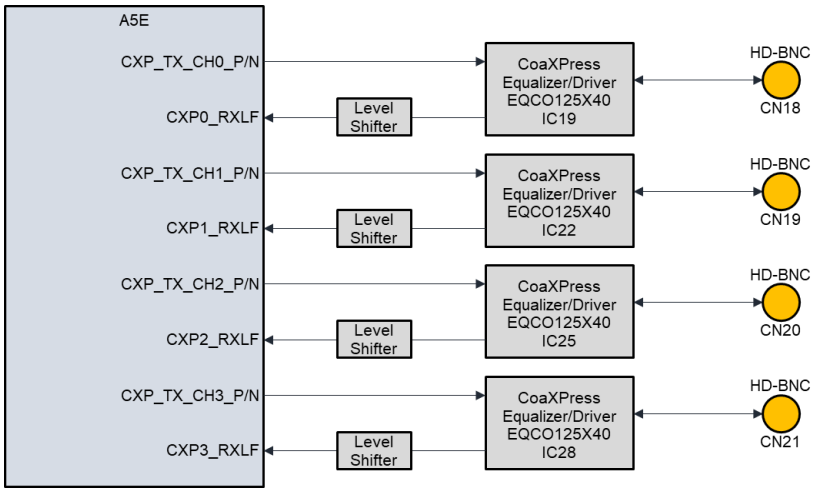


Figure 2-26 CoaXPress Circuit

Table 2-17 CoaXPress Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
CXP_TX_CH2_N	CN2.B55	GTSR_4A_TX_CH2_N	BL10	High Speed Differential I/O
CXP_TX_CH2_P	CN2.B56	GTSR_4A_TX_CH2_P	BL7	High Speed Differential I/O
CXP_TX_CH0_N	CN2.B59	GTSR_4A_TX_CH0_N	BY10	High Speed Differential I/O
CXP_TX_CH0_P	CN2.B60	GTSR_4A_TX_CH0_P	BY7	High Speed Differential I/O
CXP_REFCLK_N	CN2.C61	GTSR_4A_REFCLK_CH1_N	BB21	Current Mode Logic (CML)
CXP_REFCLK_P	CN2.C62	GTSR_4A_REFCLK_CH1_P	BB16	Current Mode Logic (CML)
CXP_TX_CH3_N	CN2.D55	GTSR_4A_TX_CH3_N	BG10	High Speed Differential I/O
CXP_TX_CH3_P	CN2.D56	GTSR_4A_TX_CH3_P	BG7	High Speed Differential I/O
CXP_TX_CH1_N	CN2.D59	GTSR_4A_TX_CH1_N	BT10	High Speed Differential I/O
CXP_TX_CH1_P	CN2.D60	GTSR_4A_TX_CH1_P	BT7	High Speed Differential I/O

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
CXP3_LF_DATA	CN2.C66	HVIO_6B_IO4	BF40	1.8-V LVCMOS
CXP1_LF_DATA	CN2.D67	HVIO_6B_IO5	BE29	1.8-V LVCMOS
CXP2_LF_DATA	CN2.C65	HVIO_6B_IO8	BF36	1.8-V LVCMOS
CXP0_LF_DATA	CN2.C68	HVIO_6B_IO9	BF29	1.8-V LVCMOS

2.13. **PCIe**

Figure 2-27 shows the board layout of PCIe on this product, Figure 2-28 shows the circuit block, Table 2-18 lists the pin assignment.

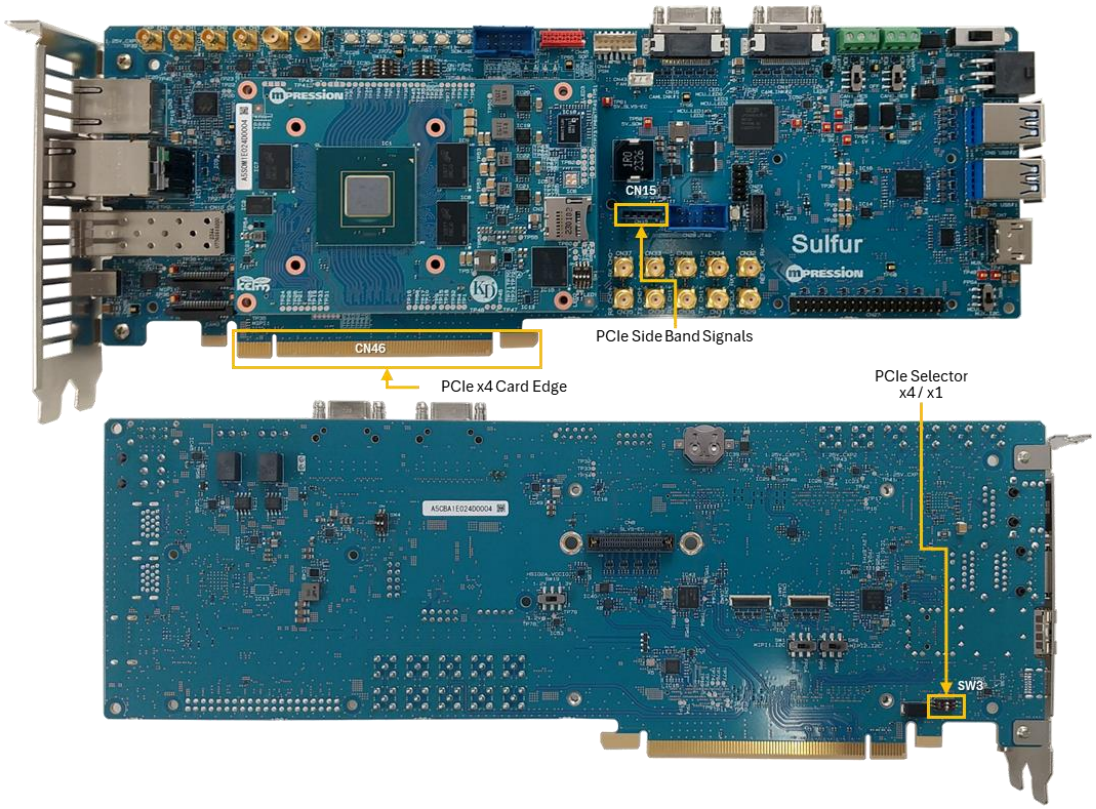


Figure 2-27 PCIe Layout

Note: The PCIe link width supported by this product is up to x4, but the physical shape of the PCIe card edge is x16. Therefore, when evaluating PCIe, please use a host board with the x16 slots.

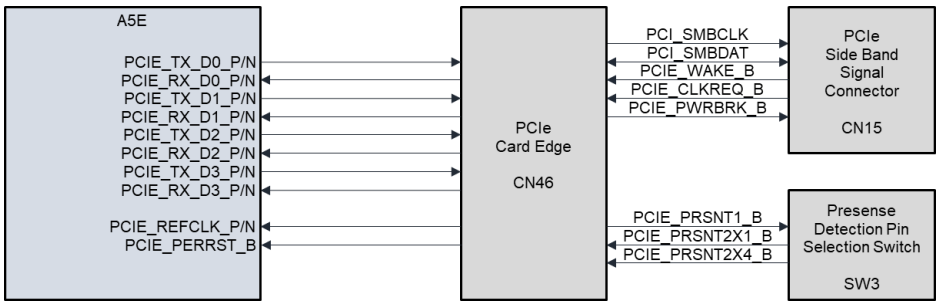


Figure 2-28 PCIe Circuit

Table 2-18 PCIe Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
PCIE_TX_D3_P	CN1.A54	GTSL_1A_TX_CH3_P	BG129	High Speed Differential I/O
PCIE_TX_D3_N	CN1.A53	GTSL_1A_TX_CH3_N	BG126	High Speed Differential I/O
PCIE_TX_D2_P	CN1.C54	GTSL_1A_TX_CH2_P	BL129	High Speed Differential I/O
PCIE_TX_D2_N	CN1.C53	GTSL_1A_TX_CH2_N	BL126	High Speed Differential I/O
PCIE_TX_D1_P	CN1.A58	GTSL_1A_TX_CH1_P	BT129	High Speed Differential I/O
PCIE_TX_D1_N	CN1.A57	GTSL_1A_TX_CH1_N	BT126	High Speed Differential I/O
PCIE_TX_D0_P	CN1.C58	GTSL_1A_TX_CH0_P	BY129	High Speed Differential I/O
PCIE_TX_D0_N	CN1.C57	GTSL_1A_TX_CH0_N	BY126	High Speed Differential I/O
PCIE_RX_D3_P	CN1.B56	GTSL_1A_RX_CH3_P	BF135	High Speed Differential I/O
PCIE_RX_D3_N	CN1.B55	GTSL_1A_RX_CH3_N	BF133	High Speed Differential I/O
PCIE_RX_D2_P	CN1.D56	GTSL_1A_RX_CH2_P	BJ135	High Speed Differential I/O
PCIE_RX_D2_N	CN1.D55	GTSL_1A_RX_CH2_N	BJ133	High Speed Differential I/O
PCIE_RX_D1_P	CN1.B60	GTSL_1A_RX_CH1_P	BN135	High Speed Differential I/O
PCIE_RX_D1_N	CN1.B59	GTSL_1A_RX_CH1_N	BN133	High Speed Differential I/O
PCIE_RX_D0_P	CN1.D60	GTSL_1A_RX_CH0_P	BV135	High Speed Differential I/O
PCIE_RX_D0_N	CN1.D59	GTSL_1A_RX_CH0_N	BV133	High Speed Differential I/O
PCIE_REFCLK_P	CN1.A62	GTSL_1A_REFCLK_CH1_P	BB120	Current Mode Logic (CML)
PCIE_REFCLK_N	CN1.A61	GTSL_1A_REFCLK_CH1_N	BB115	Current Mode Logic (CML)
PCIE_PERST_B	CN2.C92	HVIO_5B_IO5	BF107	3.3-V LVCMOS

2.13.1. **PCIe Sideband Signals Connector (CN15)**

This is the connector for PCIe sideband signals input / output. If necessary, connect it to the 40-pin Header using lead wires.

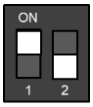
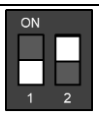
Table 2-19 PCIe Sideband Signals Connector Pin Assignments

Pin No.	Signal Name	Description
1	PCIE_SMBCLK	SMBus interface clock signal
2	PCIE_SMDAT	SMBus interface address / data signal
3	PCIE_WAKE_B	PCIe WAKE# signal
4	PCIE_CLKREQ_B	PCIe CLKREQ# signal
5	PCIE_PWRBRK_B	PCIe PWRBRK# signal

2.13.2. **PCIe Card PRSNT2# Signal Selection (SW3)**

Allows you to select the PRSNT2# signal to connect to the PRSNT1# signal for the PCIe Card presence detection function.

Table 2-20 PCIe Card PRSNT2# Signal Selection Switch

Reference	Name	Description	Drawing
SW3.1	PRSNT2X1_B	When SW3.2 is OFF and this switch is turned ON, x1 side PRSTN2 connects to PRSTN1#	
SW3.2	PRSNT2X4_B	When SW3.1 is OFF and this switch is turned ON, x4 side PRSTN2 connects to PRSTN1# (Default)	

Note: Please use this setting as the default.

2.14. **CAN**

Figure 2-29 shows the board layout of CAN on this product, Figure 2-30 shows the circuit block, Table 2-21 lists the pin assignment. This product is equipped with the MCU that implements a CAN protocol stack and communicates with the FPGA via SPI.

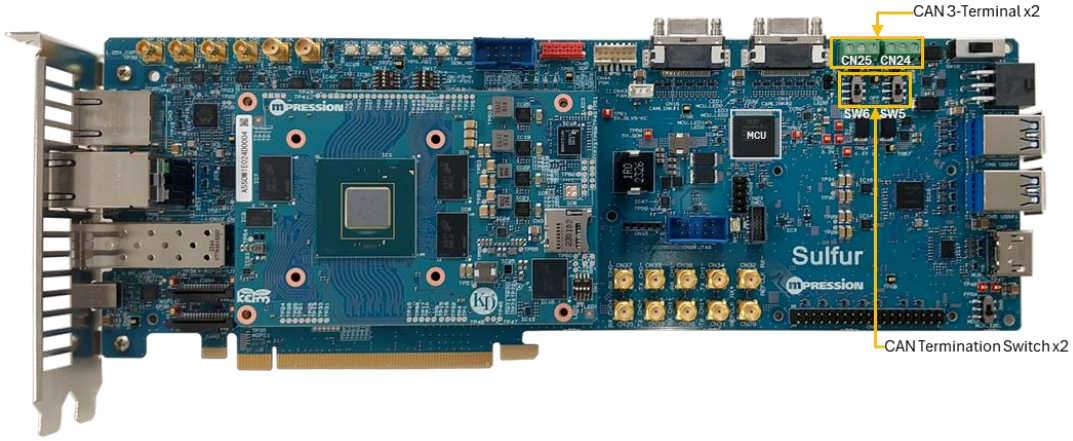


Figure 2-29 CAN Layout

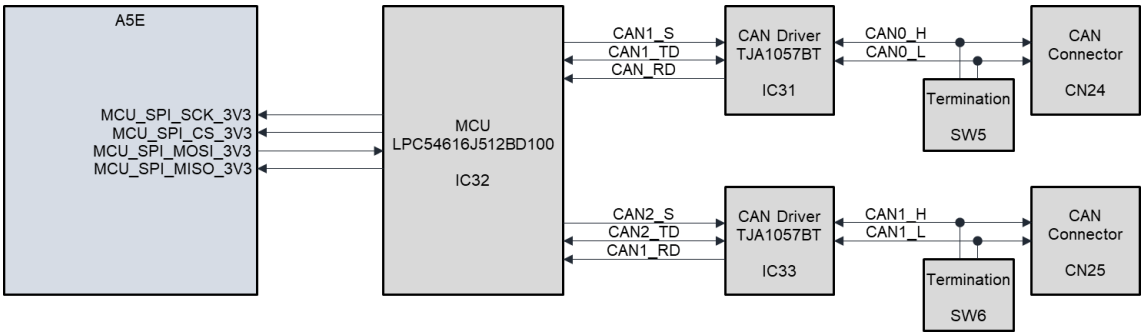


Figure 2-30 CAN Circuit

Table 2-21 CAN Circuit Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
MCU_SPI_MOSI_3V3	CN2.A93	HVIO_5A_IO18	CL130	3.3-V LVCMOS
MCU_SPI_CS_3V3	CN2.A95	HVIO_5A_IO5	CH132	3.3-V LVCMOS
MCU_SPI_SCK_3V3	CN2.B93	HVIO_5A_IO8	CK134	3.3-V LVCMOS
MCU_SPI_MISO_3V3	CN2.B96	HVIO_5A_IO6	CF132	3.3-V LVCMOS

2.14.1. **CAN Connector (CN24, CN25)**

Connector Part Number: 691214310003 (WE)

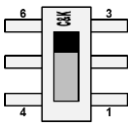
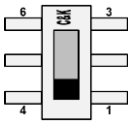
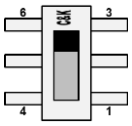
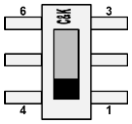
Connector Specifications: 3-Terminals, Screw

Applicable Wire: AWG24~AWG16

Pin No.	Signal Name	Description
1	CAN_H	CAN_H Bus Line
2	CAN_L	CAN_L Bus Line
3	GND	Ground

2.14.2. **CAN Termination Selection Switch (SW5, SW6)**

Table 2-22 CAN Termination Selection Switch

Reference	Name	Description	Drawing
SW5	CAN1 Termination Select	3, 6 side: Turn ON the Terminal (Default)	
		1, 4 side: Turn OFF the Terminal	
SW6	CAN2 Termination Select	3, 6 side: Turn ON the Terminal (Default)	
		1, 4 side: Turn OFF the Terminal	

2.15. **MCU**

Figure 2-31 shows the board layout of MCU on this product.

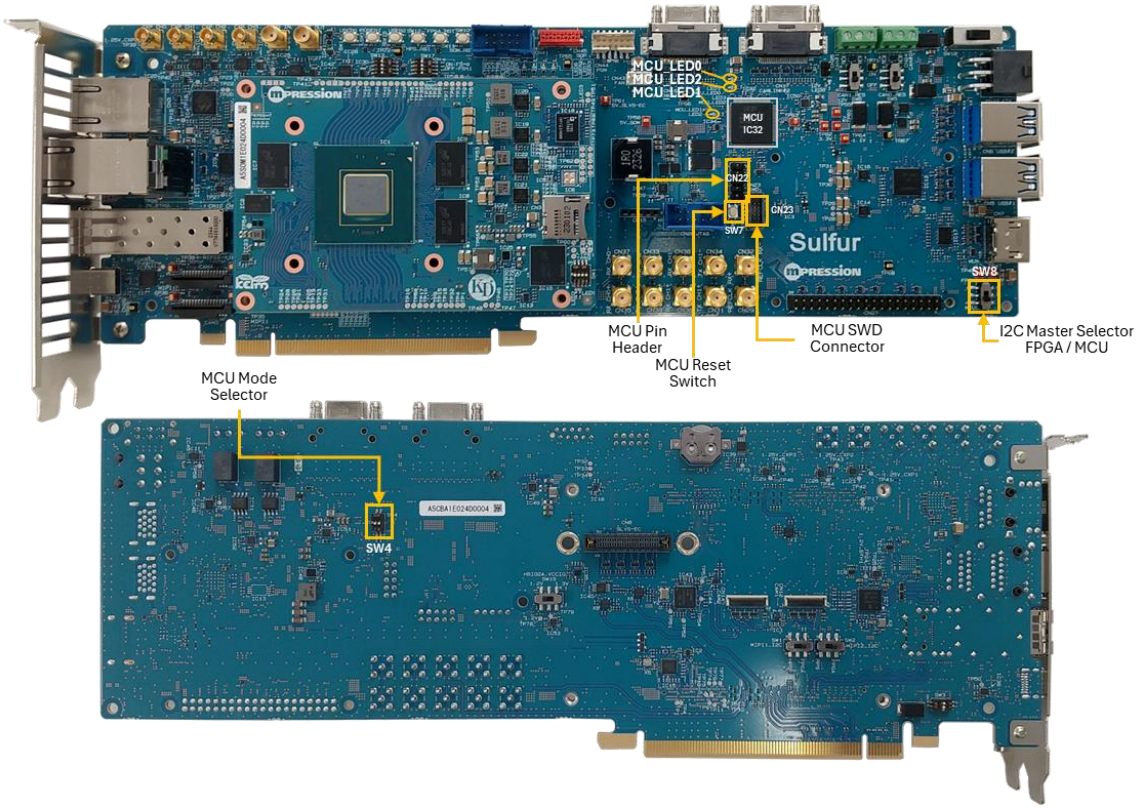


Figure 2-31 MCU Layout

2.15.1. **MCU Status LED**

Table 2-23 MCU Status LED

Reference	Nam	Description
LED1	MCU_LED0	Signal Monitor for FPGA Status 1 ON: CONF_DONE=High OFF: CONF_DONE=Low
LED2	MCU_LED1	Signal Monitor for FPGA Status 2 ON: INIT_DONE=High OFF: INIT_DONE=Low
LED3	MCU_LED2	Signal Monitor for MCU (Heartbeat) Blink: Program running ON or OFF: Program stopped

2.15.2. **SWD Connector (CN23)**

The SWD Connector allows you to evaluate or verify the MCU on this product. When evaluating or verifying, connect the MCU-Link Debug Probe to the SWD Connector and use the MCUXpresso as the software tool.

For details the MCU-Link Debug Probe and the MCUXpresso, please see below.

MCU-Link Debug Probe
https://www.nxp.jp/design/design-center/software/development-software/mcuxpresso-software-and-tools-/mcu-link-debug-probe:MCU-LINK

MCUXpresso
https://www.nxp.jp/design/design-center/software/development-software/mcuxpresso-software-and-tools-:MCUXPRESSO

2.15.3. **MCU Mode Switch (SW4)**

Table 2-24 MCU Mode Switch

Reference	Name	Description
SW4.1	MCU_ISP0	ON: ISP enable, set when writing built-in Flash
		OFF: ISP disable, boot from built-in Flash (Default)
SW4.2	MCU_GPIO0_17	ON：User Switch, set GPIO0_17 to Low (Default)
		OFF：User Switch, set GPIO0_17 to High

2.15.4. **MCU Pin Header (CN22)**

The MCU Pin Header allow you to observe signals during MCU evaluation and verification. In the sample project, pins 3 and 4 are used for serial terminal connection, pins 5 to 10 are connected to ADCs and GPIOs but are unused and reserved pins.

Table 2-25 MCU Pin Header

Pin No.	Signal Name	Description
1	3.3V	3.3V-Power
2	GND	Ground
3	MCU_UART_TXD_3V3	MCU UART Transmit Date
4	MCU_UART_RXD_3V3	MCU UART Receiver Data
5	MCU_ADC0_4	MCU ADC0_4
6	MCU_GPIO1_21_3V3	MCU GPIO1_21
7	MCU_ADC0_5	MCU ADC0_5
8	MCU_GPIO1_28_3V3	MCU GPIO1_28
9	MCU_ADC0_6	MCU ADC0_6
10	MCU_GPIO1_29_3V3	MCU GPIO1_29

2.16. **USB-UART**

Figure 2-32 shows the board layout of USB-UART Connector on this product, Figure 2-33 shows the circuit block, Table 2-26 lists the pin assignment.

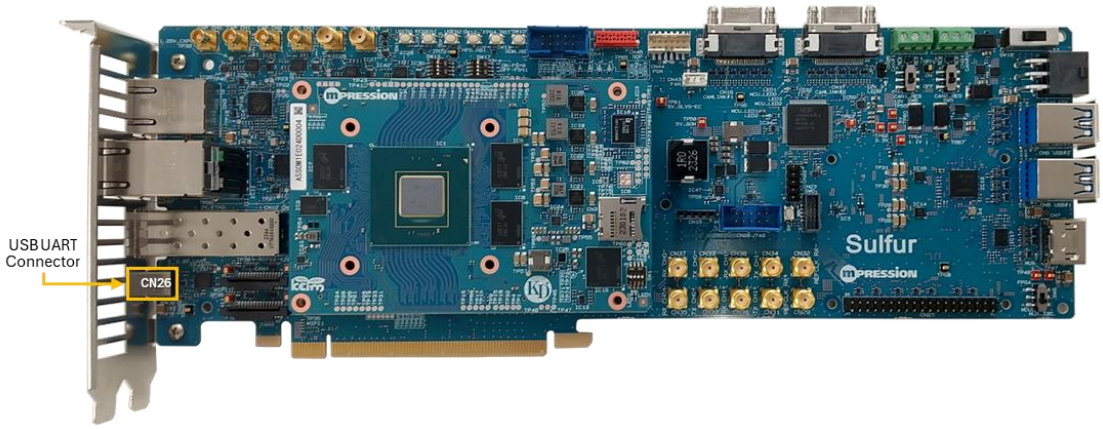


Figure 2-32 USB-UART Connector Layout

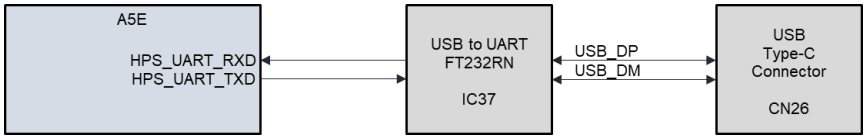


Figure 2-33 UART Circuit

Table 2-26 UART Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
HPS_UART_TXD	CN1.A17	HPS_UART_TXD	W134	1.8-V LVCMOS
HPS_UART_RXD	CN1.A18	HPS_UART_RXD	AK115	1.8-V LVCMOS

2.17. **SMA Connector**

Figure 2-34 shows the board layout of the SMA Connector on this product, Figure 2-35 shows the circuit block , Table 2-27 lists the pin assignment.

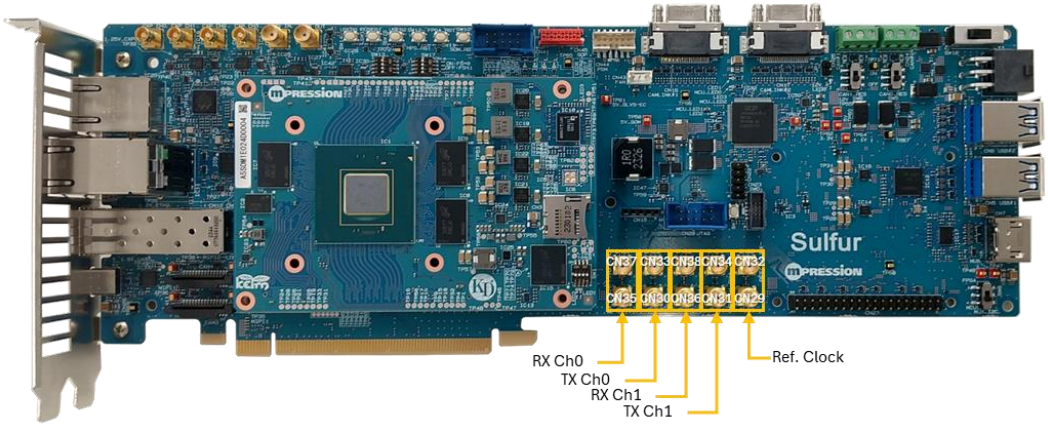


Figure 2-34 SMA Connector Layout

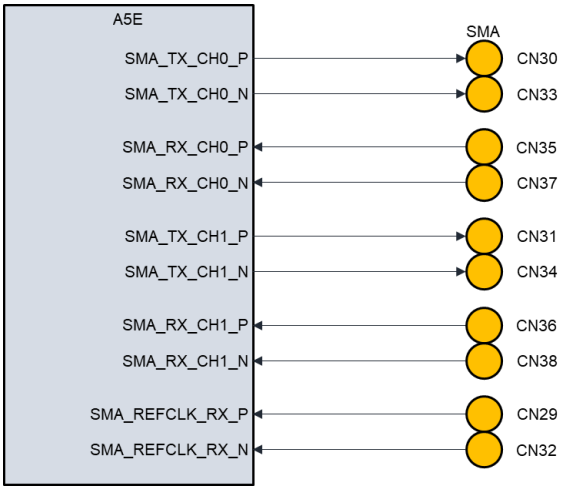


Figure 2-35 SMA Circuit

Table 2-27 SMA Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
SMA_TX_CH1_N	CN1.A37	GTSL_1C_TX_CH1_N	AR126	High Speed Differential I/O
SMA_TX_CH1_P	CN1.A38	GTSL_1C_TX_CH1_P	AR129	High Speed Differential I/O
SMA_RX_CH1_N	CN1.B39	GTSL_1C_RX_CH1_N	AP133	High Speed Differential I/O
SMA_RX_CH1_P	CN1.B40	GTSL_1C_RX_CH1_P	AP135	High Speed Differential I/O
SMA_TX_CH0_N	CN1.C37	GTSL_1C_TX_CH0_N	AU126	High Speed Differential I/O
SMA_TX_CH0_P	CN1.C38	GTSL_1C_TX_CH0_P	AU129	High Speed Differential I/O
SMA_RX_CH0_N	CN1.D39	GTSL_1C_RX_CH0_N	AT133	High Speed Differential I/O
SMA_RX_CH0_P	CN1.D40	GTSL_1C_RX_CH0_P	AT135	High Speed Differential I/O
SMA_REFCLK_RX_N	CN1.D51	GTSL_1B_REFCLK_RX_N	AY115	Current Mode Logic (CML)
SMA_REFCLK_RX_P	CN1.D52	GTSL_1B_REFCLK_RX_P	AY120	Current Mode Logic (CML)

2.18. **I2C Circuit**

Figure 2-36 shows the I2C Circuit on this product, Table 2-28 lists the pin assignment.

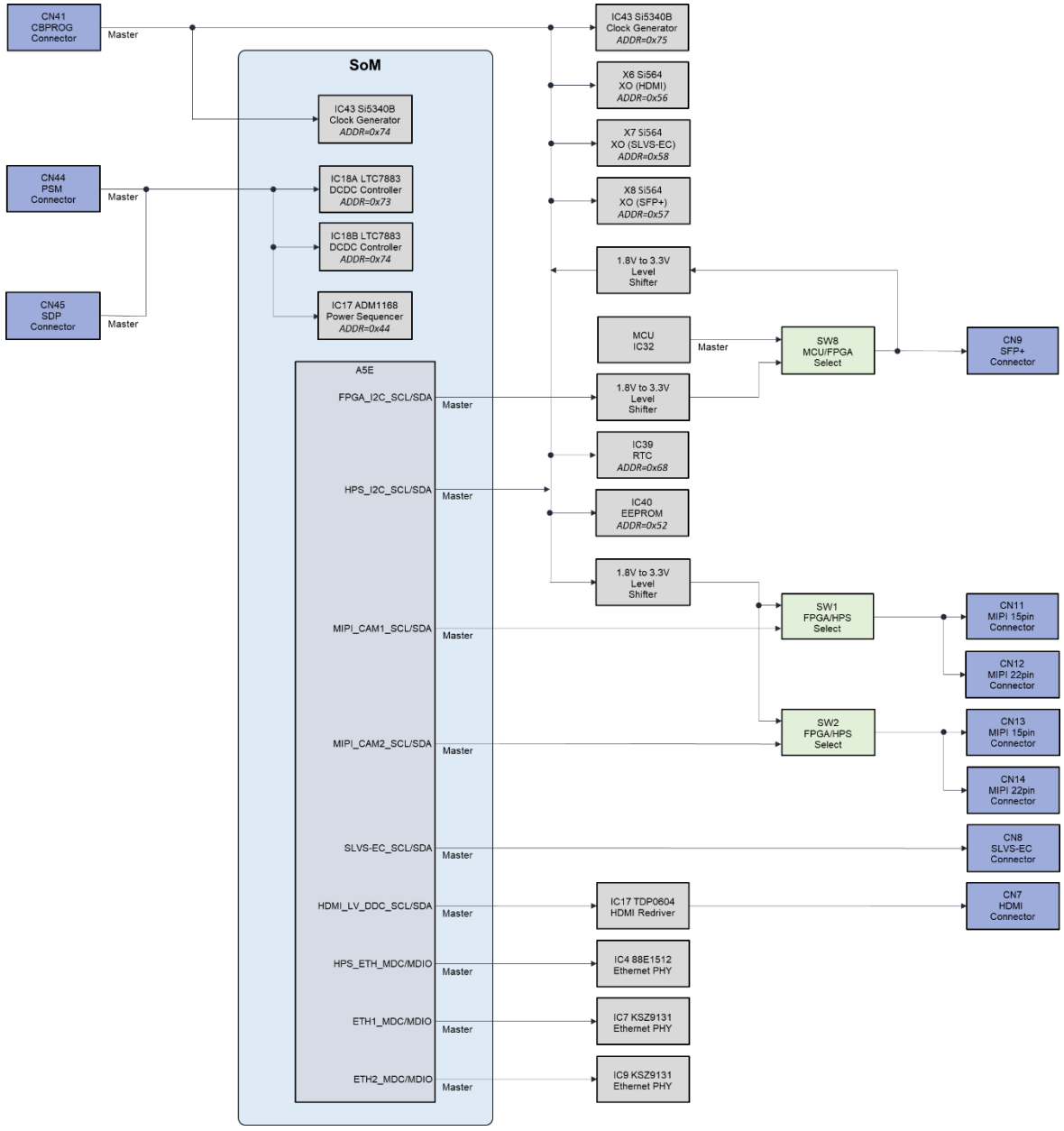


Figure 2-36 I2C Circuit

Table 2-28 I2C Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
SLVS-EC_SDI_SDA_1V8	CN2.B72	HVIO_6A_IO14	BU22	1.8-V LVCMOS
SLVS-EC_SCK_SCL_1V8	CN2.A71	HVIO_6A_IO1	BU28	1.8-V LVCMOS
MIPI_CAM2_SDA_3V3	CN2.B81	HVIO_5A_IO13	BU118	3.3-V LVCMOS
MIPI_CAM2_SCL_3V3	CN2.B82	HVIO_5A_IO14	BR118	3.3-V LVCMOS
MIPI_CAM1_SDA_3V3	CN2.A83	HVIO_5A_IO7	CF128	3.3-V LVCMOS
MIPI_CAM1_SCL_3V3	CN2.B84	HVIO_5A_IO11	CF121	3.3-V LVCMOS
HPS_I2C_SDA_1V8	CN1.C18	HPS_I2C_SDA_1V8	N135	1.8 V

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
HPS_I2C_SCL_1V8	CN1.C17	HPS_I2C_SCL_1V8	AK120	1.8 V
HPS_ETH_MDIO	CN1.D16	HPS_ETH_MDIO	R134	1.8 V
HPS_ETH_MDC	CN1.D17	HPS_ETH_MDC	AG115	1.8 V
HDMI_LV_DDC_SDA_3V3	CN2.A96	HVIO_5A_IO17	CL128	3.3-V LVCMOS
HDMI_LV_DDC_SCL_3V3	CN2.B97	HVIO_5A_IO20	CK128	3.3-V LVCMOS
FPGA_I2C_SDA_1V8	CN2.A77	HVIO_6A_IO5	BU31	1.8-V LVCMOS
FPGA_I2C_SCL_1V8	CN2.A78	HVIO_6A_IO8	BM31	1.8-V LVCMOS
ETH2_MDIO	CN2.C26	HVIO_6C_IO12	H8	1.8-V LVCMOS
ETH2_MDC	CN2.C27	HVIO_6C_IO10	K8	1.8-V LVCMOS
ETH1_MDIO	CN2.A14	HVIO_6D_IO18	B35	1.8-V LVCMOS
ETH1_MDC	CN2.B20	HVIO_6D_IO12	B26	1.8-V LVCMOS

2.19. **Debug Interface**

This product is equipped with various debugging connectors for evaluating and verifying devices on the board, Figure 2-37 shows the board layout of the Debug I/F Connector.

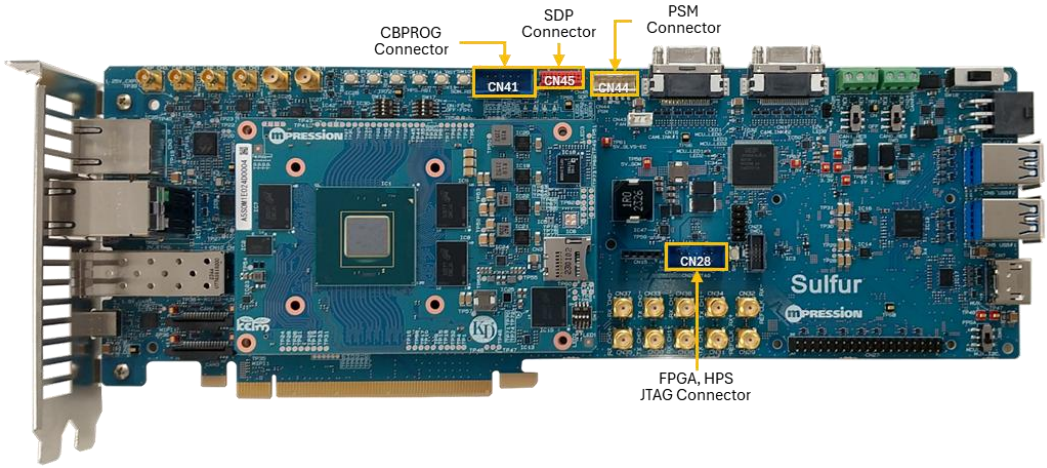


Figure 2-37 Debug I/F Connector Layout

2.19.1. **JTAG Connector (CN28)**

The JTAG Connector allows you to evaluate and verify the FPGA on the SoM of this product. To use the feature, connect the Intel® FPGA Download Cable II. Figure 2-38 shows the JTAG Circuit of this product.

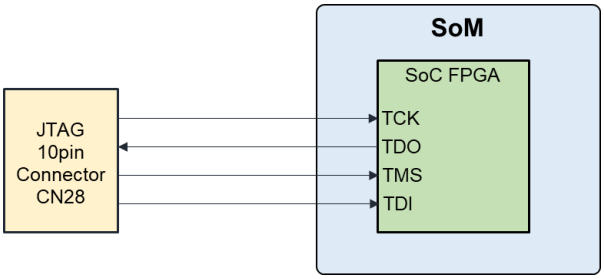


Figure 2-38 JTAG Circuit

For details the Intel® FPGA Download Cable II, please see below.

- Intel® FPGA Download Cable II
https://www.intel.co.jp/content/www/jp/ja/products/sku/215664/intel-fpga-download-cable-ii/specifications.html

2.19.2. **CBPROG Connector (CN41)**

The CBPROG Connector allows you to change settings such as the frequency of the clock generator Si5340B (Skyworks) on this product. To use this feature, connect the CBPROG-DONGLE to the CBPROG Connector and use the ClockBuilder Pro Software as the software tool.

For details the CBPROG-DONGLE and the ClockBuilder Pro Software, please see below.

- CBPROG-DONGLE
  https://www.skyworksinc.com/ja-jp/products/timing/evaluation%20kits/general/clockbuilder-pro-field-programmer/

- ClockBuilder Pro Software (CBPro)
  https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software

2.19.3. **PSM Connector (CN44)**

The PSM Connector allows to you to connect to the Power Controller LTC7883 (ADI) on the SoM of this product to monitor the voltage or currents of each power supply. To use this feature, connect the DC1613A to the PSM Connector and use the LTpowerPlay® as the software tool.

For details the DC1613A and the LTpowerPlay®, please see below.

- DC1613A
  https://www.analog.com/jp/resources/evaluation-hardware-and-software/evaluation-boards-kits/dc1613a.html

- LTpowerPlay®
  https://www.analog.com/jp/lp/ltpower-play.html

2.19.4. **SDP Connector (CN45)**

The SDP Connector allows to you to connect to the Power Sequencer ADM1168 (ADI) on the SoM of this product to set the power supply or reset sequence. To use this feature, connect the USB-SDP-CABLEZ to the SDP Connector and use the SuperSequncer evaluation software as software tool.

For details the USB-SDP-CABLEZ and the SuperSequncer evaluation software, please see below.

- USB-SDP-CABLEZ
  https://www.analog.com/jp/resources/evaluation-hardware-and-software/evaluation-boards-kits/eval_usb-sdp-cablez.html

- SuperSequncer evaluation software
  https://www.analog.com/jp/resources/evaluation-hardware-and-software/evaluation-boards-kits/eval-adm1168.html#eb-overview

2.20. **User Interface**

Figure 2-39 shows the board layout of this product, Figure 2-40 shows the circuit block, Table 2-29 lists the pin assignment.

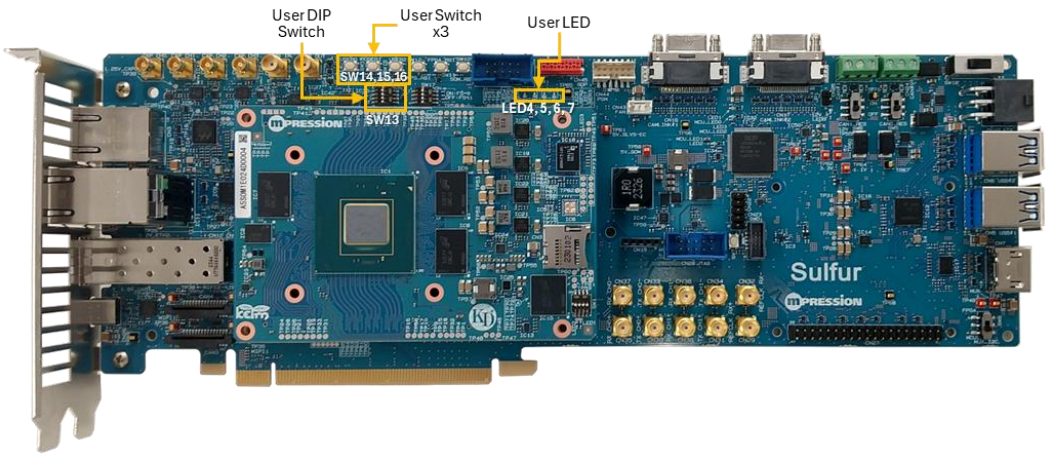


Figure 2-39 User Interface Layout

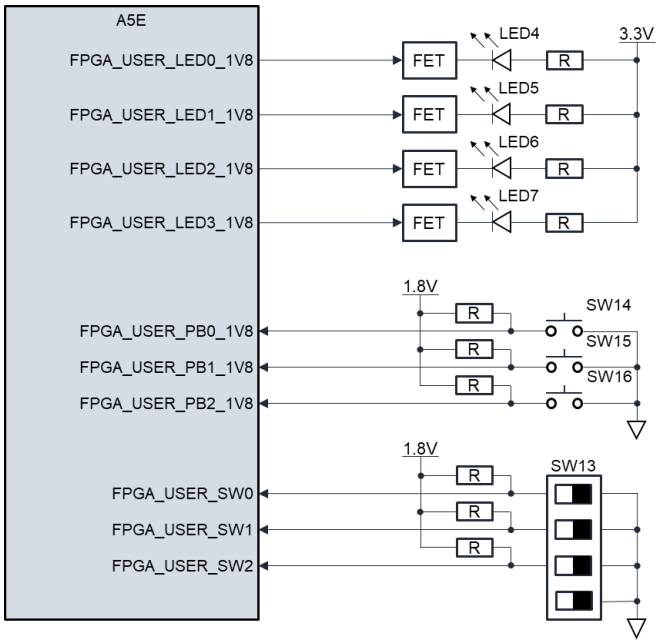


Figure 2-40 User Interface Circuit

Table 2-29 User Interface Pin Assignments

Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	I/O Standard
FPGA_USER_LED0_1V8	CN2.D16	HVIO_6C_IO4	D24	1.8-V LVCMOS
FPGA_USER_LED1_1V8	CN2.C14	HVIO_6C_IO2	F24	1.8-V LVCMOS
FPGA_USER_LED2_1V8	CN2.D13	HVIO_6C_IO3	H27	1.8-V LVCMOS
FPGA_USER_LED3_1V8	CN2.D14	HVIO_6C_IO1	F27	1.8-V LVCMOS
FPGA_USER_PB0_1V8	CN2.B78	HVIO_6A_IO4	BR31	1.8-V LVCMOS
FPGA_USER_PB1_1V8	CN2.A75	HVIO_6A_IO2	BP31	1.8-V LVCMOS
FPGA_USER_PB2_1V8	CN2.B75	HVIO_6A_IO16	BH28	1.8-V LVCMOS
FPGA_USER_SW0	CN2.A27	HVIO_6D_IO2	B4	1.8-V LVCMOS
FPGA_USER_SW1	CN2.A26	HVIO_6D_IO1	A8	1.8-V LVCMOS
FPGA_USER_SW2	CN2.B25	HVIO_6D_IO3	A11	1.8-V LVCMOS

2.20.1. **User LED**

Table 2-30 User LED

Reference	Name	Description
LED4	FPGA_USER_LED0	Turns OFF when the signal is set to Low (logic 0), turns ON when the signal is set to High (logic 1)
LED5	FPGA_USER_LED1	Turns OFF when the signal is set to Low (logic 0), turns ON when the signal is set to High (logic 1)
LED6	FPGA_USER_LED2	Turns OFF when the signal is set to Low (logic 0), turns ON when the signal is set to High (logic 1)
LED7	FPGA_USER_LED3	Turns OFF when the signal is set to Low (logic 0), turns ON when the signal is set to High (logic 1)

2.20.2. **User Push Switches**

Table 2-31 User Push Switches

Reference	Name	Description
SW14	FPGA_USER_PB0	Low (logic 0) when the switch is pressed, otherwise High (logic 1)
SW15	FPGA_USER_PB1	Low (logic 0) when the switch is pressed, otherwise High (logic 1)
SW16	FPGA_USER_PB2	Low (logic 0) when the switch is pressed, otherwise High (logic 1)

2.20.3. **User DIP Switch**

Table 2-32 User DIP Switch

Reference	Name	Description
SW13	FPGA_USER_SW0	Low (logic 0) when the switch is turned ON, High (logic 1) when the switch is turn OFF.
	FPGA_USER_SW1	Low (logic 0) when the switch is turned ON, High (logic 1) when the switch is turn OFF.
	FPGA_USER_SW2	Low (logic 0) when the switch is turned ON, High (logic 1) when the switch is turn OFF.

2.21. **40-Pin Header (CN27)**

Figure 2-41 shows the board layout of this product, Table 2-33 lists the pin assignment.

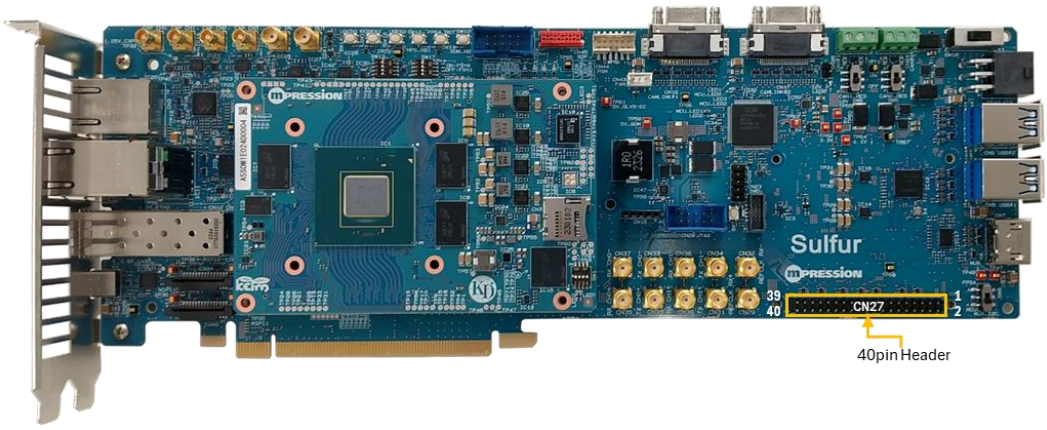


Figure 2-41 40-Pin Header Layout

Table 2-33 40-Pin Header Pin Assignments

Pin No.	Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	Description
1	3.3V	-	-	-	3.3V Output
2	5V	-	-	-	5V Output
3	USER_GPIO2	CN2.C78	HVIO_6B_IO17	CK2	3.3-V LVCMOS
4	5V	-	-	-	5V Output
5	USER_GPIO3	CN2.D78	HVIO_6B_IO20	CH4	3.3-V LVCMOS
6	GND	-	-	-	Ground
7	USER_GPIO4	CN2.C75	HVIO_6B_IO15	BU19	3.3-V LVCMOS
8	USER_GPIO14	CN2.D70	HVIO_6B_IO7	BF32	3.3-V LVCMOS
9	GND	-	-	-	Ground
10	USER_GPIO15	CN2.C93	HVIO_5B_IO15	BM118	3.3-V LVCMOS
11	USER_GPIO17	CN2.D94	HVIO_5B_IO19	BH118	3.3-V LVCMOS
12	USER_GPIO18	CN2.C87	HVIO_5B_IO7	BF104	3.3-V LVCMOS
13	USER_GPIO27	CN2.D84	HVIO_5B_IO6	BU109	3.3-V LVCMOS
14	GND	-	-	-	Ground
15	USER_GPIO22	CN2.D88	HVIO_5B_IO12	BM109	3.3-V LVCMOS
16	USER_GPIO23	CN2.C86	HVIO_5B_IO13	BR112	3.3-V LVCMOS
17	3.3V	-	-	-	3.3V Output
18	USER_GPIO24	CN2.D85	HVIO_5B_IO16	BP112	3.3-V LVCMOS
19	USER_GPIO10	CN2.C72	HVIO_6B_IO1	BF21	3.3-V LVCMOS
20	GND	-	-	-	Ground
21	USER_GPIO9	CN2.C71	HVIO_6B_IO11	BF16	3.3-V LVCMOS
22	USER_GPIO25	CN2.C83	HVIO_5B_IO10	BK109	3.3-V LVCMOS
23	USER_GPIO11	CN2.D72	HVIO_6B_IO2	BE21	3.3-V LVCMOS
24	USER_GPIO8	CN2.D73	HVIO_6B_IO13	BK22	3.3-V LVCMOS
25	GND	-	-	-	Ground
26	USER_GPIO7	CN2.C74	HVIO_6B_IO12	BH19	3.3-V LVCMOS
27	USER_GPIO0	CN2.D79	HVIO_6B_IO19	CK4	3.3-V LVCMOS
28	USER_GPIO1	CN2.C77	HVIO_6B_IO18	CJ2	3.3-V LVCMOS
29	USER_GPIO5	CN2.D75	HVIO_6B_IO16	BR19	3.3-V LVCMOS
30	GND	-	-	-	Ground
31	USER_GPIO6	CN2.D76	HVIO_6B_IO14	BM19	3.3-V LVCMOS
32	USER_GPIO12	CN2.C69	HVIO_6B_IO10	BF25	3.3-V LVCMOS
33	USER_GPIO13	CN2.D69	HVIO_6B_IO6	BE25	3.3-V LVCMOS
34	GND	-	-	-	Ground
35	USER_GPIO19	CN2.C90	HVIO_5B_IO17	BM112	3.3-V LVCMOS
36	USER_GPIO16	CN2.D93	HVIO_5B_IO14	BK118	3.3-V LVCMOS
37	USER_GPIO26	CN2.C84	HVIO_5B_IO8	BR109	3.3-V LVCMOS

Pin No.	Signal Name	BtoB Pin	SoM Pin Name	A5E Pin	Description
38	USER_GPIO20	CN2.C89	HVIO_5B_IO18	BK112	3.3-V LVCMOS
39	GND	-	-	-	Ground
40	USER_GPIO21	CN2.D87	HVIO_5B_IO2	BH109	3.3-V LVCMOS

3. SoM Connector

Figure 3-1 shows the board layout of the SoM Connector used to connect with the SoM.

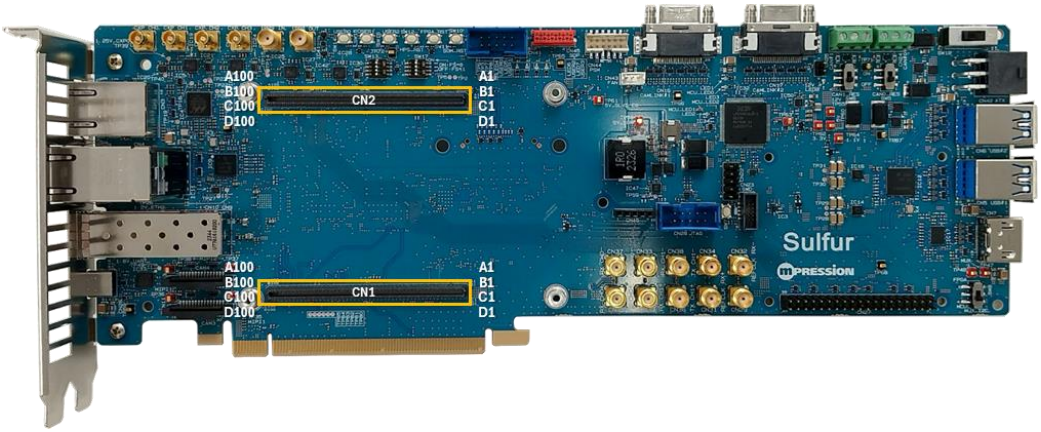


Figure 3-1 SoM Connector Layout

3.1. CN1 Pin Assignments

Table 3-1 CN1 Pin Assignments

Pin No.	Row A	Row B	Row C	Row D
1	5V_SOM	5V_SOM	5V_SOM	5V_SOM
2	5V_SOM	5V_SOM	5V_SOM	5V_SOM
3	5V_SOM	5V_SOM	5V_SOM	5V_SOM
4	GND	5V_SOM	GND	5V_SOM
5	HPS_ULPI_DATA5	5V_SOM	SOM_RSVD	5V_SOM
6	HPS_ULPI_DATA3	GND	SOM_RSVD	GND
7	GND	HPS_ULPI_DATA2	GND	HPS_RGMII_TX_CLK
8	HPS_ULPI_DATA7	HPS_ULPI_DATA6	HPS_RGMII_RX_CLK	HPS_RGMII_TX_CTRL
9	HPS_ULPI_DATA1	GND	HPS_RGMII_RX_CTRL	GND
10	GND	HPS_ULPI_DATA4	GND	HPS_RGMII_TXD0
11	HPS_ULPI_DATA0	HPS_ULPI_CLK	HPS_RGMII_RXD0	HPS_RGMII_TXD1
12	HPS_ULPI_NXT	GND	HPS_RGMII_RXD1	GND
13	GND	HPS_ULPI_STP	GND	HPS_RGMII_TXD2
14	SOM_RST_OUT_B_1V8	HPS_ULPI_DIR	HPS_RGMII_RXD2	HPS_RGMII_TXD3
15	-	GND	HPS_RGMII_RXD3	GND
16	GND	HPS_INT_B_1V8	GND	HPS_ETH_MDIO
17	HPS_UART_TXD	-	HPS_I2C_SCL_1V8	HPS_ETH_MDC
18	HPS_UART_RXD	GND	HPS_I2C_SDA_1V8	GND
19	GND	HPS_1PPS_OUT_1V8	GND	HPS_ETH_INT_B
20	-	HPS_1PPS_IN_1V8	-	-
21	-	GND	-	GND
22	GND	-	GND	SOM_RSVD
23	-	-	-	SOM_RSVD
24	-	GND	TP	GND
25	GND	-	GND	-
26	-	-	-	TP
27	-	GND	-	GND
28	GND	SOM_JTAG_TDO_1V8	GND	TP
29	SOM_PMBUS_SDA_3V3	SOM_JTAG_TMS_1V8	TP	TP
30	SOM_PMBUS_SCL_3V3	GND	TP	GND
31	GND	SOM_JTAG_TDI_1V8	GND	-
32	GND	SOM_JTAG_TCK_1V8	GND	TP
33	SFP_TXD_N	GND	USB3_UP_TXD_N	GND
34	SFP_TXD_P	GND	USB3_UP_TXD_P	GND
35	GND	SFP_RXD_N	GND	USB3_UP_RXD_N
36	GND	SFP_RXD_P	GND	USB3_UP_RXD_P
37	SMA_TX_CH1_N	GND	SMA_TX_CH0_N	GND

Pin No.	Row A	Row B	Row C	Row D
38	SMA_TX_CH1_P	GND	SMA_TX_CH0_P	GND
39	GND	SMA_RX_CH1_N	GND	SMA_RX_CH0_N
40	GND	SMA_RX_CH1_P	GND	SMA_RX_CH0_P
41	USB3_REFCLK_N	GND	SFP_REFCLK_N	GND
42	USB3_REFCLK_P	GND	SFP_REFCLK_P	GND
43	GND	HDMI_TX_CLK_N	GND	HDMI_TX_DATA2_N
44	GND	HDMI_TX_CLK_P	GND	HDMI_TX_DATA2_P
45	pulldown	GND	pulldown	GND
46	pulldown	GND	pulldown	GND
47	GND	HDMI_TX_DATA1_N	GND	HDMI_TX_DATA0_N
48	GND	HDMI_TX_DATA1_P	GND	HDMI_TX_DATA0_P
49	pulldown	GND	pulldown	GND
50	pulldown	GND	pulldown	GND
51	GND	HDMI_REFCLK_N	GND	SMA_REFCLK_RX_N
52	GND	HDMI_REFCLK_P	GND	SMA_REFCLK_RX_P
53	PCIE_TX_D3_N	GND	PCIE_TX_D2_N	GND
54	PCIE_TX_D3_P	GND	PCIE_TX_D2_P	GND
55	GND	PCIE_RX_D3_N	GND	PCIE_RX_D2_N
56	GND	PCIE_RX_D3_P	GND	PCIE_RX_D2_P
57	PCIE_TX_D1_N	GND	PCIE_TX_D0_N	GND
58	PCIE_TX_D1_P	GND	PCIE_TX_D0_P	GND
59	GND	PCIE_RX_D1_N	GND	PCIE_RX_D0_N
60	GND	PCIE_RX_D1_P	GND	PCIE_RX_D0_P
61	PCIE_REFCLK_N	GND	pulldown	GND
62	PCIE_REFCLK_P	GND	pulldown	GND
63	GND	-	GND	MIPI_CAM3_D1_N
64	GND	RZQ	GND	MIPI_CAM3_D1_P
65	CAM_LINK2_XCLK_N	GND	CAM_LINK2_SERTC_N	GND
66	CAM_LINK2_XCLK_P	CAM_LINK2_X0_N	CAM_LINK2_SERTC_P	MIPI_CAM3_D0_N
67	GND	CAM_LINK2_X0_P	GND	MIPI_CAM3_D0_P
68	CAM_LINK2_X1_N	GND	CAM_LINK2_SERTFG_N	GND
69	CAM_LINK2_X1_P	CAM_LINK2_X3_N	CAM_LINK2_SERTFG_P	MIPI_CAM3_C_N
70	GND	CAM_LINK2_X3_P	GND	MIPI_CAM3_C_P
71	CAM_LINK2_CC3_N	GND	CAM_LINK2_CC1_N	GND
72	CAM_LINK2_CC3_P	CAM_LINK2_X2_N	CAM_LINK2_CC1_P	-
73	GND	CAM_LINK2_X2_P	GND	-
74	MIPI_CAM4_D1_N	GND	CAM_LINK2_CC4_N	GND
75	MIPI_CAM4_D1_P	MIPI_CAM4_D0_N	CAM_LINK2_CC4_P	-
76	GND	MIPI_CAM4_D0_P	GND	-
77	MIPI_CAM4_C_N	GND	CAM_LINK2_CC2_N	GND
78	MIPI_CAM4_C_P	-	CAM_LINK2_CC2_P	-
79	GND	-	GND	-
80	-	GND	-	GND
81	-	CAM_LINK1_X0_N	-	1.2V_SOM
82	GND	CAM_LINK1_X0_P	GND	1.2V_SOM
83	MIPI_REFCLK_N	GND	MIPI_CAM1_D0_N	GND
84	MIPI_REFCLK_P	CAM_LINK1_X1_N	MIPI_CAM1_D0_P	MIPI_CAM2_D1_N
85	GND	CAM_LINK1_X1_P	GND	MIPI_CAM2_D1_P
86	CAM_LINK1_XCLK_N	GND	MIPI_CAM1_D1_N	GND
87	CAM_LINK1_XCLK_P	CAM_LINK1_X2_N	MIPI_CAM1_D1_P	MIPI_CAM2_D0_N
88	GND	CAM_LINK1_X2_P	GND	MIPI_CAM2_D0_P
89	CAM_LINK1_CC3_N	GND	MIPI_CAM1_C_N	GND
90	CAM_LINK1_CC3_P	CAM_LINK1_X3_N	MIPI_CAM1_C_P	MIPI_CAM2_C_N
91	GND	CAM_LINK1_X3_P	GND	MIPI_CAM2_C_P
92	CAM_LINK1_CC4_N	GND	MIPI_CAM1_D3_N	GND
93	CAM_LINK1_CC4_P	CAM_LINK1_SERTC_N	MIPI_CAM1_D3_P	MIPI_CAM2_D2_N
94	GND	CAM_LINK1_SERTC_P	GND	MIPI_CAM2_D2_P
95	CAM_LINK1_SERTFG_N	GND	MIPI_CAM1_D2_N	GND
96	CAM_LINK1_SERTFG_P	-	MIPI_CAM1_D2_P	MIPI_CAM2_D3_N
97	GND	-	GND	MIPI_CAM2_D3_P
98	CAM_LINK1_CC1_N	GND	-	GND
99	CAM_LINK1_CC1_P	CAM_LINK1_CC2_N	-	1.2V_SOM
100	GND	CAM_LINK1_CC2_P	GND	1.2V_SOM

3.2. CN2 Pin Assignments

Table 3-2 CN2 Pin Assignments

Pin No.	Row A	Row B	Row C	Row D
1	5V_SOM	5V_SOM	5V_SOM	5V_SOM
2	5V_SOM	5V_SOM	5V_SOM	5V_SOM
3	5V_SOM	5V_SOM	5V_SOM	5V_SOM
4	GND	5V_SOM	GND	5V_SOM
5	SOM_RSVD	5V_SOM	SOM_RSVD	5V_SOM
6	SOM_RSVD	GND	SOM_RSVD	GND
7	GND	SOM_FPGA_RESET_TRG_1V8	GND	SOM_RSVD
8	SOM_RESET_B_1V8	SOM_HPS_RESET_TRG_1V8	SOM_CLKG_SCL_1V8	SOM_RSVD
9	SOM_PWR_OK	GND	SOM_CLKG_SDA_1V8	GND
10	GND	SOM_PWR_EN_1V8	GND	1.8V_VBAT
11	1.8V_SOM	-	-	-
12	1.8V_SOM	GND	-	GND
13	GND	ETH1_INT_B	GND	FPGA_USER_LED2_1V8
14	ETH1_MDIO	ETH1_RGMII_TX_CTRL	FPGA_USER_LED1_1V8	FPGA_USER_LED3_1V8
15	ETH1_RGMII_TX_CLK	GND	ETH2_RGMII_RXD3	GND
16	GND	ETH1_RGMII_TXD0	GND	FPGA_USER_LED0_1V8
17	ETH1_RGMII_TXD1	ETH1_RGMII_TXD3	ETH2_RGMII_RXD0	ETH2_RGMII_RXD2
18	ETH1_RGMII_TXD2	GND	ETH2_RGMII_RXD1	GND
19	GND	ETH1_RGMII_RX_CLK	GND	ETH2_RGMII_RX_CLK
20	HVIO_6D_REFCLK_1V8	ETH1_MDC	ETH2_RGMII_TXD3	ETH2_RGMII_RX_CTRL
21	ETH1_RGMII_RX_CTRL	GND	ETH2_RGMII_TXD1	GND
22	GND	ETH1_RGMII_RXD0	GND	ETH2_RGMII_TXD2
23	ETH1_RGMII_RXD1	ETH1_RGMII_RXD3	ETH2_RGMII_TX_CTRL	ETH2_INT_B
24	ETH1_RGMII_RXD2	GND	ETH2_RGMII_TX_CLK	GND
25	GND	FPGA_USER_SW2	GND	ETH2_RGMII_TXD0
26	FPGA_USER_SW1	ETH1_RESET_B	ETH2_MDIO	ETH2_RESET_B
27	FPGA_USER_SW0	GND	ETH2_MDC	GND
28	GND	-	GND	1.8V_SOM
29	-	-	-	1.8V_SOM
30	-	GND	-	GND
31	GND	-	GND	-
32	GND	-	GND	-
33	SLVS-EC_RX_CH6_N	GND	SLVS-EC_RX_CH7_N	GND
34	SLVS-EC_RX_CH6_P	GND	SLVS-EC_RX_CH7_P	GND
35	GND	-	GND	-
36	GND	-	GND	-
37	SLVS-EC_RX_CH4_N	GND	SLVS-EC_RX_CH5_N	GND
38	SLVS-EC_RX_CH4_P	GND	SLVS-EC_RX_CH5_P	GND
39	GND	-	GND	-
40	GND	-	GND	-
41	pulldown	GND	pulldown	GND
42	pulldown	GND	pulldown	GND
43	GND	SLVS-EC_RX_CH2_N	GND	SLVS-EC_RX_CH3_N
44	GND	SLVS-EC_RX_CH2_P	GND	SLVS-EC_RX_CH3_P
45	-	GND	-	GND
46	-	GND	-	GND
47	GND	SLVS-EC_RX_CH0_N	GND	SLVS-EC_RX_CH1_N
48	GND	SLVS-EC_RX_CH0_P	GND	SLVS-EC_RX_CH1_P
49	-	GND	-	GND
50	-	GND	-	GND
51	GND	SLVS-EC_REFCLK_N	GND	pulldown
52	GND	SLVS-EC_REFCLK_P	GND	pulldown
53	pulldown	GND	pulldown	GND
54	pulldown	GND	pulldown	GND
55	GND	CXP_TX_CH2_N	GND	CXP_TX_CH3_N
56	GND	CXP_TX_CH2_P	GND	CXP_TX_CH3_P
57	pulldown	GND	pulldown	GND
58	pulldown	GND	pulldown	GND
59	GND	CXP_TX_CH0_N	GND	CXP_TX_CH1_N
60	GND	CXP_TX_CH0_P	GND	CXP_TX_CH1_P
61	pulldown	GND	CXP_REFCLK_N	GND
62	pulldown	GND	CXP_REFCLK_P	GND

Pin No.	Row A	Row B	Row C	Row D
63	GND	-	GND	-
64	GND	-	GND	-
65	SLVS-EC_XTRIG2_1V8	GND	CXP2_LF_DATA	GND
66	SLVS-EC_XTRIG1_1V8	SLVS-EC_XVS_1V8	CXP3_LF_DATA	FAN_PULSE
67	GND	SLVS-EC_XMASTER_1V8	GND	CXP1_LF_DATA
68	SLVS-EC_XHS_1V8	GND	CXP0_LF_DATA	GND
69	SLVS-EC_SDO_1V8	SLVS-EC_XCE_1V8	USER_GPIO12	USER_GPIO13
70	GND	SLVS-EC_XCLR_1V8	GND	USER_GPIO14
71	SLVS-EC_SCK_SCL_1V8	GND	USER_GPIO9	GND
72	SLVS-EC_SENSOR_PON_1V8	SLVS-EC_SDI_SDA_1V8	USER_GPIO10	USER_GPIO11
73	GND	SLVS-EC_SENSOR_PGOOD_1V8	GND	USER_GPIO8
74	SLVS-EC_OMODE_1V8	GND	USER_GPIO7	GND
75	FPGA_USER_PB1_1V8	FPGA_USER_PB2_1V8	USER_GPIO4	USER_GPIO5
76	GND	SLVS-EC_INCK_OE_1V8	GND	USER_GPIO6
77	FPGA_I2C_SDA_1V8	GND	USER_GPIO1	GND
78	FPGA_I2C_SCL_1V8	FPGA_USER_PB0_1V8	USER_GPIO2	USER_GPIO3
79	GND	HVIO_6A_REFCLK_1V8	GND	USER_GPIO0
80	1.8V_SOM	GND	-	GND
81	1.8V_SOM	MIPI_CAM2_SDA_3V3	-	3.3V_SOM
82	GND	MIPI_CAM2_SCL_3V3	GND	3.3V_SOM
83	MIPI_CAM1_SDA_3V3	GND	USER_GPIO25	GND
84	MIPI_CAM2_GPIO1_3V3	MIPI_CAM1_SCL_3V3	USER_GPIO26	USER_GPIO27
85	GND	MIPI_CAM2_GPIO0_3V3	GND	USER_GPIO24
86	MIPI_CAM1_GPIO1_3V3	GND	USER_GPIO23	GND
87	-	USB_ID_3V3	USER_GPIO18	USER_GPIO21
88	GND	MIPI_CAM1_GPIO0_3V3	GND	USER_GPIO22
89	3.3V_SOM	GND	USER_GPIO20	GND
90	3.3V_SOM	-	USER_GPIO19	3.3V_SOM
91	GND	-	GND	3.3V_SOM
92	USB_VBUS_DET_3V3	GND	PCIE_PERST_B	GND
93	MCU_SPI_MOSI_3V3	MCU_SPI_SCK_3V3	USER_GPIO15	USER_GPIO16
94	GND	-	GND	USER_GPIO17
95	MCU_SPI_CS_3V3	GND	SFP_RATE_SEL1	GND
96	HDMI_LV_DDC_SDA_3V3	MCU_SPI_MISO_3V3	SFP_TX_DISABLE	SFP_TX_FAULT
97	GND	HDMI_LV_DDC_SCL_3V3	GND	SFP_RATE_SEL0
98	SOM_RSVD	GND	SFP_MOD_ABS	GND
99	SOM_RSVD	HDMI_EN_3V3	SFP_LOS	SOM_RSVD
100	GND	HDMI_HPD_3V3	GND	SOM_RSVD

3.3. Signal Mames and Descriptions

Table 3-3 SoM Connector Signal Names and Descriptions

Signal Name	Dir (Carrier)	Voltage	SoM Connect	Description
5V_SOM	Out	5V	Power Circuit	5V Power Supply
3.3V_SOM	Out	3.3V	3.3V Bank	3.3V VCCIO Voltage
1.2V_SOM	Out	1.2V or 1.3V	HSIO_2A	1.1V VCCIO Voltage
1.8V_SOM	Out	1.8V	1.8V Bank	1.8V VCCIO Voltage
1.8V_VBAT	Out	1.8V	VCCBAT	Battery backup for AES
GND	-	-	GND	Ground
RZQ	In	-	HSIO_2A_B	Reference resistor 240-Ohm for OCT
pulldown	pulldown	-	-	Connect to GND via a resistor for input-only pin processing
TP	N/C	-	-	Reserved pin, not connected on board.
SOM_RSVD	N/C	-	-	Reserved pin, not connected on board.
HPS_ULPI_DATA[7:0]	I/O	1.8V	HPS	USB ULPI Data Bus
HPS_ULPI_CLK	Out	1.8V	HPS	USB ULPI Clock
HPS_ULPI_NXT	Out	1.8V	HPS	USB ULPI NXT Signal
HPS_ULPI_STP	In	1.8V	HPS	USB ULPI STP Signal
HPS_ULPI_DIR	Out	1.8V	HPS	USB ULPI DIR Signal
HPS_RGMII_TX_CLK	In	1.8V	HPS	Ethernet (HPS) RGMII Transmit Clock
HPS_RGMII_TX_CTRL	In	1.8V	HPS	Ethernet (HPS) RGMII Transmit Control
HPS_RGMII_TXD[3:0]	In	1.8V	HPS	Ethernet (HPS) RGMII Transmit Data
HPS_RGMII_RX_CLK	Out	1.8V	HPS	Ethernet (HPS) RGMII Receive Clock

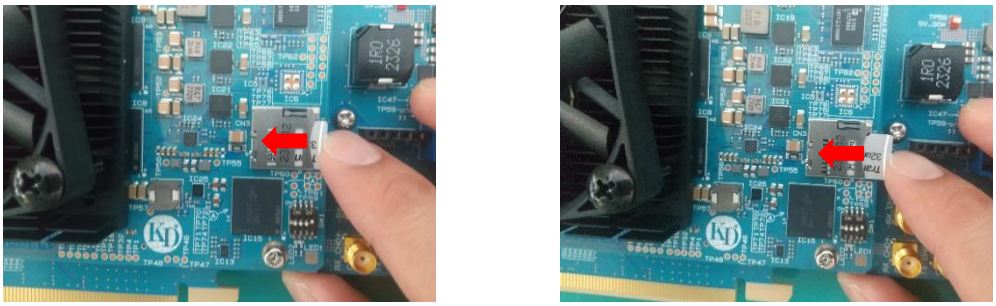
Signal Name	Dir (Carrier)	Voltage	SoM Connect	Description
HPS_RGMII_RX_CTRL	Out	1.8V	HPS	Ethernet (HPS) RGMII Receive Control
HPS_RGMII_RXD[3:0]	Out	1.8V	HPS	Ethernet (HPS) RGMII Receive Data
HPS_ETH_MDIO	I/O	1.8V	HPS	Ethernet (HPS) PHY Management Data
HPS_ETH_MDC	In	1.8V	HPS	Ethernet (HPS) PHY Management Clock
HPS_ETH_INT_B	Out	1.8V	HPS	Ethernet (HPS) PHY Interrupt
SOM_RST_OUT_B_1V8	Out	1.8V	Reset Circuit	SoM Reset Output
HPS_UART_TXD	Out	1.8V	HPS	UART Transmit Data
HPS_UART_RXD	In	1.8V	HPS	UART Receive Data
HPS_I2C_SCL_1V8	In	1.8V	HPS	I2C Clock
HPS_I2C_SDA_1V8	I/O	1.8V	HPS	I2C Data
HPS_1PPS_OUT_1V8	In	1.8V	HPS	TSN Sync Signal
HPS_1PPS_IN_1V8	Out	1.8V	HPS	TSN Sync Signal
SOM_JTAG_TCLK_1V8	Out	1.8V	JTAG	JTAG Test Clock
SOM_JTAG_TMS_1V8	Out	1.8V	JTAG	JTAG Test Select
SOM_JTAG_TDO_1V8	In	1.8V	JTAG	JTAG Test Data Output
SOM_JTAG_TDI_1V8	Out	1.8V	JTAG	JTAG Test Data Input
SOM_PMBUS_SDA_3V3	I/O	3.3V	電源回路	PMBus Data
SOM_PMBUS_SCL_3V3	Out	3.3V	電源回路	PMBus Clock
SOM_CLKG_SCL_1V8	Out	1.8V	クロック回路	I2C Clock (Clock Generator)
SOM_CLKG_SDA_1V8	I/O	1.8V	クロック回路	I2C Data (Clock Generator)
SOM_RESET_B_1V8	Out	1.8V	電源回路	Re-Config Request
SOM_FPGA_RESET_TRG_1V8	Out	1.8V	電源回路	FPGA Reset Request
SOM_HPS_RESET_TRG_1V8	Out	1.8V	電源回路	HPS Reset Request
SOM_PWR_OK	In	1.8V	電源回路	SoM Power OK
SOM_PWR_EN	Out	1.8V	電源回路	SoM Power Enable
SFP_TXD_[P/N]	In	1.0V	GTSL_1C	10GbE Transmit Data
SFP_RXD_[P/N]	Out	1.0V	GTSL_1C	10GbE Receive Data
SFP_REFCLK_[P/N]	Out	1.0V	GTSL_1C	10GbE Reference Clock
SFP_RATE_SEL[n]	In	3.3V	HVIO_5B	10GbE Rate Select: n is a number (0-1)
SFP_TX_DISABLE	In	3.3V	HVIO_5B	10GbE Transmit Disable Signal
SFP_MOD_ABS	Out	3.3V	HVIO_5B	10GbE MOD_ABS Signal
SFP_LOS	Out	3.3V	HVIO_5B	10GbE Receive Los Signal
SFP_TX_FAULT	Out	3.3V	HVIO_5B	10GbE Transmit Fault Signal
USB3_UP_TXD_[P/N]	In	1.0V	GTSL_1C	USB3.1 Transmit Data
USB3_UP_RXD_[P/N]	Out	1.0V	GTSL_1C	USB3.1 Receive Data
USB3_REFCLK_[P/N]	Out	1.0V	GTSL_1C	USB3.1 Reference Clock
HDMI_TX_CLK_[P/N]	In	1.0V	GTSL_1B	HDMI Clock
HDMI_TX_DATA[n]_[P/N]	In	1.0V	GTSL_1B	HDMI Data: n is a number (0-2)
HDMI_REFCLK_[P/N]	Out	1.0V	GTSL_1B	HDMI Reference Clock
PCIE_TX_D[n]_[P/N]	In	1.0V	GTSL_1A	PCIe Transmit Data: n is a number (0-3)
PCIE_RX_D[n]_[P/N]	Out	1.0V	GTSL_1A	PCIe Receive Data: n is a number (0-3)
PCIE_REFCLK_[P/N]	Out	1.0V	GTSL_1A	PCIe Reference Clock
PCIE_PERST_B	Out	3.3V	HVIO_5B	PCIe Reset
SMA_TX_CH[n]_[P/N]	In	1.0V	GTSL_1C	SMA Connected Transceiver Transmit Data: n is a number (0-1)
SMA_RX_CH[n]_[P/N]	Out	1.0V	GTSL_1C	SMA Connected Transceiver Receive Data: n is a number (0-1)
SMA_REFCLK_RX_[P/N]	Out	1.0V	GTSL_1B	SMA Connected Transceiver Reference Clock
SLVS-EC_RX_CH[n]_[P/N]	Out	1.0V	GTSR_4C GTSR_4B	SLVS-EC Data Lane: n is a number (0-7)
SLVS-EC_REFCLK_[P/N]	Out	1.0V	GTSR_4B	SLVS-EC Reference Clock
SLVS-EC_XCLR_1V8	In	1.8V	HVIO_6A	SLVS-EC XCLR
SLVS-EC_INCK_OE_1V8	In	1.8V	HVIO_6A	SLVS-EC INCK_OE
SLVS-EC_XVS_1V8	In	1.8V	HVIO_6A	SLVS-EC INCK_OE
SLVS-EC_XHS_1V8	In	1.8V	HVIO_6A	SLVS-EC XVS
SLVS-EC_XTRIG1_1V8	In	1.8V	HVIO_6A	SLVS-EC XHS
SLVS-EC_XTRIG2_1V8	In	1.8V	HVIO_6A	SLVS-EC XTRIG1
SLVS-EC_SCK_SCL_1V8	In	1.8V	HVIO_6A	SLVS-EC XTRIG2
SLVS-EC_XCE_1V8	In	1.8V	HVIO_6A	SLVS-EC SCK_SCL
SLVS-EC_SDI_SDA_1V8	I/O	1.8V	HVIO_6A	SLVS-EC XCE
SLVS-EC_SDO_1V8	Out	1.8V	HVIO_6A	SLVS-EC SDI_SDA
SLVS-EC_XMASTER_1V8	In	1.8V	HVIO_6A	SLVS-EC XMASTER
SLVS-EC_OMODE_1V8	In	1.8V	HVIO_6A	SLVS-EC OMODE
SLVS-EC_SENSOR_PON_1V8	In	1.8V	HVIO_6A	SLVS-EC SENSOR_PON
SLVS-EC_SENSOR_PGOOD_1V8	Out	1.8V	HVIO_6A	SLVS-EC SENSOR_PGOOD
HVIO_6A_REFCLK_1V8	Out	1.8V	HVIO_6A	Reference Clock 100MHz

Signal Name	Dir (Carrier)	Voltage	SoM Connect	Description
HVIO_6D_REFCLK_1V8	Out	1.8V	HVIO_6D	Reference Clock 100MHz
ETH1_RGMII_TX_CLK	In	1.8V	HVIO_6D	Ethernet (FPGA1) RGMII Transmit Clock
ETH1_RGMII_TX_CTRL	In	1.8V	HVIO_6D	Ethernet (FPGA1) RGMII Receive Control
ETH1_RGMII_TXD[3:0]	In	1.8V	HVIO_6D	Ethernet (FPGA1) RGMII Transmit Data
ETH1_RGMII_RX_CLK	Out	1.8V	HVIO_6D	Ethernet (FPGA1) RGMII Receive Clock
ETH1_RGMII_RX_CTRL	Out	1.8V	HVIO_6D	Ethernet (FPGA1) RGMII Receive Control
ETH1_RGMII_RXD[3:0]	Out	1.8V	HVIO_6D	Ethernet (FPGA1) RGMII Receive Data
ETH1_MDIO	I/O	1.8V	HVIO_6D	Ethernet (FPGA1) PHY Management Data
ETH1_MDC	In	1.8V	HVIO_6D	Ethernet (FPGA1) PHY Management Clock
ETH1_INT_B	Out	1.8V	HVIO_6D	Ethernet (FPGA1) PHY Interrupt
ETH1_RESET_B	In	1.8V	HVIO_6D	Ethernet (FPGA1) PHY Reset
ETH2_RGMII_TX_CLK	In	1.8V	HVIO_6D	Ethernet (FPGA2) RGMII Transmit Clock
ETH2_RGMII_TX_CTRL	In	1.8V	HVIO_6D	Ethernet (FPGA2) RGMII Transmit Control
ETH2_RGMII_TXD[3:0]	In	1.8V	HVIO_6D	Ethernet (FPGA2) RGMII Transmit Data
ETH2_RGMII_RX_CLK	Out	1.8V	HVIO_6D	Ethernet (FPGA2) RGMII Receive Clock
ETH2_RGMII_RX_CTRL	Out	1.8V	HVIO_6D	Ethernet (FPGA2) RGMII Receive Control
ETH2_RGMII_RXD[3:0]	Out	1.8V	HVIO_6D	Ethernet (FPGA2) RGMII Receive Data
ETH2_MDIO	I/O	1.8V	HVIO_6D	Ethernet (FPGA2) PHY Management Data
ETH2_MDC	In	1.8V	HVIO_6D	Ethernet (FPGA2) PHY Management Clock
ETH2_INT_B	Out	1.8V	HVIO_6D	Ethernet (FPGA2) PHY Interrupt
ETH2_RESET_B	In	1.8V	HVIO_6D	Ethernet (FPGA2) PHY Reset
MIPI_REFCLK	Out	1.2V	HSIO_2A_T	MIPI Reference Clock
MIPI_CAM1_D[n]_[P/N]	Out	1.2V	HSIO_2A_T	MIPI CAM1 Data: n is a number (0-3)
MIPI_CAM1_C_[P/N]	Out	1.2V	HSIO_2A_T	MIPI CAM1 Clock
MIPI_CAM1_SCL_3V3	In	3.3V	HVIO_5A	MIPI CAM1 I2C Clock
MIPI_CAM1_SDA_3V3	I/O	3.3V	HVIO_5A	MIPI CAM1 I2C Data
MIPI_CAM1_GPIO[n]_3V3	I/O	3.3V	HVIO_5A	MIPI CAM1 GPIO: n is a number (0-1)
MIPI_CAM2_D[n]_[P/N]	Out	1.2V	HSIO_2A_T	MIPI CAM2 Data: n is a number (0-3)
MIPI_CAM2_C_[P/N]	Out	1.2V	HSIO_2A_T	MIPI CAM2 Clock
MIPI_CAM2_SCL_3V3	In	3.3V	HVIO_5A	MIPI CAM1 I2C Clock
MIPI_CAM2_SDA_3V3	I/O	3.3V	HVIO_5A	MIPI CAM1 I2C Data
MIPI_CAM2_GPIO[n]_3V3	I/O	3.3V	HVIO_5A	MIPI CAM1 GPIO: n is a number (0-1)
MIPI_CAM3_D[n]_[P/N]	Out	1.2V	HSIO_2A_B	MIPI CAM3 Data: n is a number (0-1)
MIPI_CAM3_C_[P/N]	Out	1.2V	HSIO_2A_B	MIPI CAM3 Clock
MIPI_CAM4_D[n]_[P/N]	Out	1.2V	HSIO_2A_B	MIPI CAM4 Data: n is a number (0-1)
MIPI_CAM4_C_[P/N]	Out	1.2V	HSIO_2A_B	MIPI CAM4 Clock
CAM_LINK1_X[n]_[P/N]	Out	1.3V	HSIO_2A_T	Camera Link #1 X Data Bus: n is a number (0-3)
CAM_LINK1_XCLK_[P/N]	Out	1.3V	HSIO_2A_T	Camera Link #1 X Clock
CAM_LINK1_SERTFG_[P/N]	Out	1.3V	HSIO_2A_T	Camera Link #1 Serial to Flame Graber
CAM_LINK1_SERTC_[P/N]	In	1.3V	HSIO_2A_T	Camera Link #1 Serial to Camera
CAM_LINK1_CC[n]_[P/N]	In	1.3V	HSIO_2A_T	Camera Link #1 Camera Control: n is a number (1-4)
CAM_LINK2_X[n]_[P/N]	Out	1.3V	HSIO_2A_B	Camera Link #2 X Data Bus: n is a number (0-3)
CAM_LINK2_XCLK_[P/N]	Out	1.3V	HSIO_2A_B	Camera Link #2 X Clock
CAM_LINK2_SERTFG_[P/N]	Out	1.3V	HSIO_2A_B	Camera Link #2 Serial to Flame Graber
CAM_LINK2_SERTC_[P/N]	In	1.3V	HSIO_2A_B	Camera Link #2 Serial to Camera
CAM_LINK2_CC[n]_[P/N]	In	1.3V	HSIO_2A_B	Camera Link #2 Camera Control: n is a number (1-4)
FPGA_USER_LED[n]_1V8	In	1.8V	HVIO_6C	User LED: n is a number (0-3)
FPGA_USER_SW[n]_1V8	In	1.8V	HVIO_6D	User DIP Switch: n is a number (0-2)
FPGA_USER_PB[n]_1V8	In	1.8V	HVIO_6A	User Push Switch: n is a number (0-2)
USER_GPIO[n]	I/O	3.3V	HVIO_6B HVIO_5B	User GPIO: n is a number (0-27)

4. How to Setup

4.1. Inserting and Removing the microSD

When inserting the microSD card, insert it horizontally into the microSD card slot on the SoM as shown in Figure 4-1, and push it in the direction of the arrow until you heard click. Also, when removing the microSD card, push it in the direction of the arrow until you hear clicks, just as you did when inserting it. The microSD card will then pop up, so carefully remove it with your fingernail.



(a) Inserting the microSD　　(b) Removing the microSD

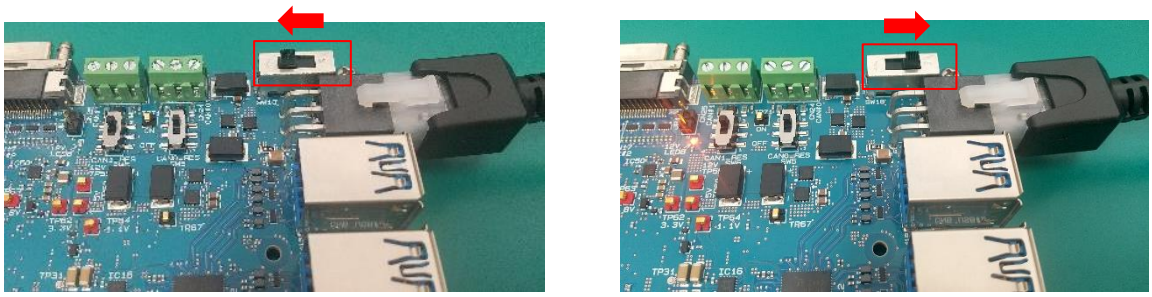
Figure 4-1 Inserting and Removing the microSD

The reference design for writing to microSD cards is available on the Sulfur website at Rocketboards.org. Please download the desired reference design and write it to the microSD card for use.

Rocketboards.org Sulfur Website:
https://www.rocketboards.org/foswiki/Documentation/MpressionSulfurDevelopmentKitForIntelAgilexR5FPGAESeries

4.2. **Power ON / OFF**

To turn on / off the power, slide the power switch (SW18) knob to the position shows in Figure 4-2. Similarly, when the power switch knob is in the power ON position, power is supplied to this board from the PCIe card edge.



(a) Power OFF (b) Power ON

Figure 4-2 Power ON / OFF

5. Board External Dimensions

Figure 4-3 shows the Board External Dimensions. (Unit: mm)

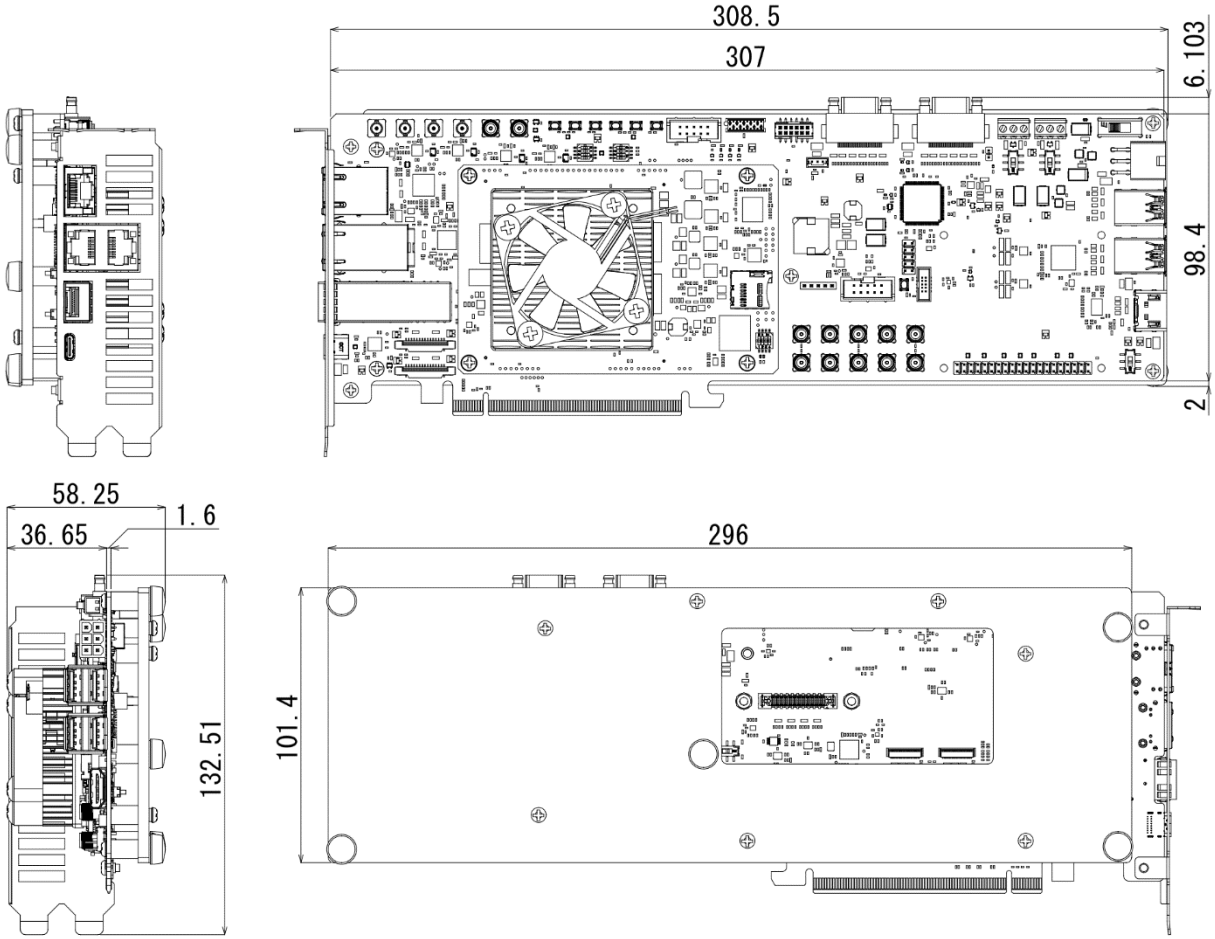


Figure 4-3 The Board External Dimensions

6. **Document History**

Ver.	Date	Changes
1.0	2024/4/24	Initial release.